International Space Power System Interoperability Standards (ISPSIS)

Revision A – July 2022

REVISION AND HISTORY

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PREFACE

INTERNATIONAL SPACE POWER SYSTEM INTEROPERABILITY STANDARDS (ISPSIS)

This electrical power quality standard is to ensure commonality, reliability, safety, interchangeability, and interoperability for electrical load applications between space power systems that will enable collaborative endeavors utilizing different spacecraft systems in deep space.

Configuration control of this document is the responsibility of the Multilateral Coordination Board (MCB). The National Aeronautics and Space Administration (NASA) will maintain the International Space Power System Interoperability Standards (ISPSIS) under Exploration Systems Development Directorate (ESDMD) Configuration Management. Any revisions to this document will be approved by the DPMC/MCB.

INTERNATIONAL SPACE POWER SYSTEM INTEROPERABILITY STANDARDS (ISPSIS)

CONCURRENCE

TBD 2022

Associate Administrator for Exploration Systems Development Mission Directorate National Aeronautics and Space Administration	Date
Executive Director of Human Space Programs State Space Corporation Roscosmos	Date
Director of Human and Robotic Exploration European Space Agency	Date
Director General, Space Exploration Canadian Space Agency	Date
Deputy Director General Research and Development Bureau Ministry of Education, Culture, Sports, Science, and Technology	Date

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1 INTRODUCTION

This International Space Power System Interoperability Standards (ISPSIS) is the result of collaborations within the International Space Station (ISS) and Gateway memberships to establish interoperable interfaces, terminology, and techniques, to facilitate collaborative endeavors of space exploration in cislunar and deep space environments. These standards are available for international and commercial partnerships.

Standards that are established and internationally recognized have been selected where possible to enable a variety of providers. Increasing hardware commonality among providers while decreasing unique configurations has the potential to reduce the traditional barriers in space exploration: overall mass and volume required to execute a mission. Standardizing interfaces reduces the scope of the development effort.

The information within this document represents a set of parameters, which if accommodated in the system architecture support greater efficiencies, promote cost savings, and increase the probability of mission success. These standards are not intended to specify system details needed for implementation nor do they dictate design features behind the interface; specific requirements will be defined in unique documents.

1.1 PURPOSE AND SCOPE

The purpose of this electrical power standard is to define bus voltages, and the associated power quality and single point grounding for individual or integrated 120 VDC and 28 VDC spacecraft power systems. These definitions will facilitate commonality, reliability, safety, interchangeability, and interoperability of load applications between space power systems such as orbital habitats, crewed or non-crewed space vehicles, ascent/descent vehicles, and surface systems. A commonality in basic equipment (lights, fans, computers, modular electrical switchgear, etc.) reduces the need for unique spares that reduce the overall spare mass allocation and required stowage volume. This has a tangible impact on module size and the ultimate mass of the launch vehicle payload.

Because this is a standard and not a specification, physical interfaces between loads and power systems are not defined.

This standard defines the requirements and characteristics of electrical power for spacecraft. These requirements and characteristics are intended to be met over the entire life of the vehicle. This standard also defines analysis, verification, and testing methodologies to be used to ensure that the loads operate when connected to the

specified power quality and performance as defined by this standard. Utilizing this power standard, a power quality specification can then be developed that includes the detailed design performance of both the Electrical Power System (EPS) and the Electrical Power Consuming Equipment (EPCE).

1.2 RESPONSIBILITY AND CHANGE AUTHORITY

Any proposed changes to this standard by the participating partners of this agreement shall be brought forward to the ISPSIS working group for review.

Configuration control of this document is the responsibility of the Multilateral Coordination Board (MCB). The National Aeronautics and Space Administration (NASA) will maintain the Power Standards under Exploration Systems Development Mission Directorate (ESDMD) Configuration Management. Any revisions to this document will be approved by the MCB.

1.3 CONVENTION AND NOTATION

This document defines its implementation of requirement verbs as follows:

a. “Shall” – Used to indicate a requirement that is binding, which must be implemented and its implementation verified in the design. Stating “The System shall” does not necessarily indicate that the System is to provide that capability, but rather the System is responsible for ensuring that the capability is being provided whether it is provided by the System directly or provided by another Gateway system or another Program.

b. “Should” – Used to indicate good practice or a goal which is desirable but not mandatory and does not require formal verification.

c. “May” – Used to indicate permission.

d. “Will” – Used to indicate a statement of fact or declaration of purpose on the part of the government that is reflective of decisions or realities that exist and are to be taken as a given and not open to debate or discussion.

e. "Is” or “Are” – Used to indicate descriptive material.

Rationales, included for many of the requirements, are intended to provide clarification, justification, purpose, and/or the source of a requirement. In the event that there is an inconsistency between a requirement and its rationale, the requirement always takes precedence.

2 DOCUMENTS

2.1 APPLICABLE DOCUMENTS

The following documents include specifications, models, standards, guidelines, handbooks, or other special publications. The documents listed in this paragraph are applicable to the extent specified herein.

None

2.2 REFERENCE DOCUMENTS

The following documents contain supplemental information to guide the user in the application of this document. These reference documents may or may not be specifically cited within the text of this document.

MIL-STD-461 G	Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment
SAE AS5698 Rev A	Space Power Standard

3 POWER QUALITY STANDARD FOR 120 VDC AND 28 VDC

3.1 GENERAL

The requirements and verifications are defined for 120 Volt and 28 Volt direct current (VDC) class power systems. 120 VDC is the Interoperability Power Standard for vehicle-to-vehicle and element-to-element interfaces, and for the vehicle's or element's power distribution to EPCE (loads). By approved exception, 28 VDC can be utilized and will be primarily utilized for lower power applications such as special purpose sub-bus distributions, portable loads, or low-power independent vehicles. The general intent is to maximize the compatibility of the EPCE across differing interfaces by broadening selected EPCE operating requirements. This standard is generic and while it can ensure compatibility on most parameters, it is limited in areas such as defining specific design impedance requirements that are needed to complete a specific design.

3.1.1 DESCRIPTION

The electrical requirements are grouped into two categories:

- Electrical Power System, Source Power Interface (section 3.3);
- Electric Power Consuming Equipment Interface (section 3.4);

Matching verifications for each of the above requirements are defined in sections 4.1 and 4.2.

3.1.2 ENGINEERING UNITS OF MEASURE

All dimensions are in the International System of Units (SI units) (metric).

3.2 INTERFACES

This standard is design-neutral and only defines the 'generic' interface of the power source and of the electric power consuming equipment and assumes it to be the same interface (see Figure 3.1.2-1: Generic Power Interface for Source/EPCE). An actual specific design may incorporate multiple interfaces both within the EPS or EPCE with tiered requirements that include performance margins above the next lower tier. The tiered interfaces with performance margins are defined within other documentation, such as the power quality specifications and the interface requirements documents.

One of the primary goals of this standard is to maximize the use of the EPCE at all defined EPCE interfaces.

The EPCE input interface is defined as the output of the primary power interface if the EPCE requires a harness, else the EPCE input interface is defined at the input terminal of the EPCE unit. For example, a laptop, which requires a harness to plug into a Portable Equipment Panel (PEP), would have its interface defined at the PEP receptacle and, therefore, the EPCE interface includes the harness. In contrast, a rack-mountable EPCE, which plugs into a fixed backplane, would have its input defined at the EPCE input terminals and, in this way, the harnessing to the EPCE is included with the source.

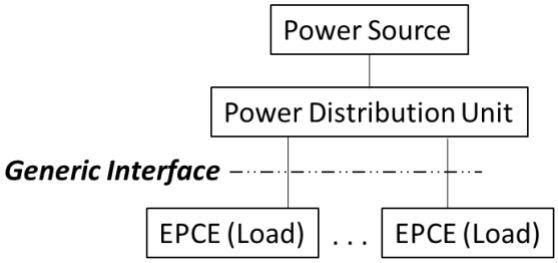


FIGURE 3.1.2-1: GENERIC POWER INTERFACE FOR SOURCE/EPCE

3.3 ELECTRICAL POWER SYSTEM, SOURCE POWER INTERFACE PERFORMANCE

The following sections specify the characteristics for electric power supplied to electrical loads.

The EPS consists of the electric power-generating source (e.g., generators, batteries, fuel cells, solar arrays, and distribution subsystems) including the associated cables, switches, protective devices, converters, and regulators.

Power quality is directly related to the effects produced by power generation, power conditioning, system impedance, and the interactions within the distribution system which includes loads. Interactions include electromagnetic interference (EMI), regenerative energy, and system transients resulting in power surges and spikes.

The requirements following a PWR120-XXXX label pertain to a 120V system and the requirements following a PWR28-XXXX label pertain to a 28V system.

3.3.1 EPS SYSTEM CHARACTERISTICS

3.3.1.1 SINGLE-POINT GROUND

PWR120-1001, PWR28-1001

A single-point ground shall be established for each EPS system.

Rationale: Establish a consistent internal grounding philosophy. This is a proven practice and consistent with heritage designs. The single-point grounding should be employed with the return lines grounded to the vehicle structure at a single point. The main characteristics of this concept are:

- *The spacecraft structure is used as a low-impedance equipotential ground plane.*
- *No current intentionally flows through the spacecraft structure.*
- *All primary power sources are referenced to a single point on the spacecraft structure.*
- *Primary power sources are galvanically isolated from secondary power supplies.*
- *Ground reference will be established for all secondary power supply outputs in order to facilitate electrical fault clearing, EMI control, and shock hazard prevention.*
- *The housing of each unit is bonded to the spacecraft structure.*

3.3.1.2 DISTRIBUTION WIRING

PWR120-1002, PWR28-1002

The EPS shall provide a two-wire power distribution system in which one wire serves as a return path for load currents.

Rationale: The wiring system is required to maintain the distributed single-point ground per requirement. The two-wire distribution system does not preclude using parallel wiring for current sharing. It is recommended to minimize spacing between power and return conductors to reduce wiring inductance. No current should intentionally flow through the spacecraft structure.

3.3.1.3 ISOLATION

PWR120-1003, PWR28-1003

EPS power distribution buses, fed from independent sources, shall be isolated.

Rationale: Isolation of power source supply and returns will be implemented such that a fault in one source will leave the other source operational. The isolation requirement is based on the distributed single-point ground and 1 Mega Ohm (MΩ) hardware configuration end item (box level) isolation requirements. No single failure within the EPS or EPCE will cause the independent power buses to lose electrical isolation. Isolation also prevents circulating alternating current (AC) or direct current (DC) in the EPS and/or spacecraft structure.

3.3.1.4 REVERSE CURRENT

PWR120-1004, PWR28-1004

The EPS shall be required to accept reverse currents from the EPCE only under abnormal operating conditions.

Rationale: Loads will be designed to prevent current to out-flow into the power system under normal load operation, on/off where the EPS voltage remains constant. Loads, mainly motors and other inertial loads, need to be designed as to not normally supply reverse currents (re-gen) into the distribution system and potentially raise the bus voltage to unacceptable levels causing the unintended tripping from other devices within the system. Ripple current is controlled by the EMI control plan.

3.3.1.5 STABILITY

Power system stability is the ability of an electric power system to return to a state of operating equilibrium within a specified time after being subjected to a physical disturbance. The EPS will remain stable over the entire range of power generation, energy storage, and load conditions in all operating modes, temperatures, and orbital phases or conditions over the power system's design life to maintain power quality. The following section addresses the requirements to assure the bus interface stability.

3.3.1.5.1 SOURCE IMPEDANCE

PWR120-1005, PWR28-1005

The EPS source impedance at the EPCE interface terminals shall be established for the power system.

Rationale: The source impedance value is required to calculate the stability margin of the source/load combination at the user input terminals. This document addresses a generic interface where the EPS and the EPCE have one common interface. Specific designs most likely will have multiple tiered interfaces between the EPS and the EPCE as discussed in paragraph 3.2 and the EPS impedance will be determined at each defined interface.

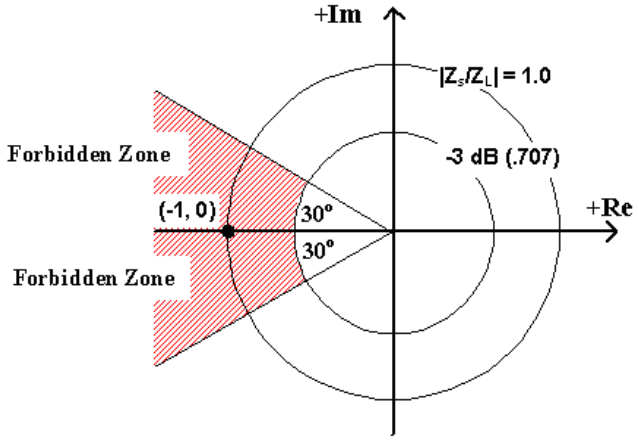
3.3.1.5.2 SMALL SIGNAL STABILITY – SYSTEM STABILITY

PWR120-1006, PWR28-1006

A complex impedance margin shall be maintained for the source impedance divided by the load impedance ratio that remains outside the hatched area (Forbidden Zone) shown in Figure 3.3.1-1: Nyquist Stability Criteria.

Rationale: This Nyquist criteria was adopted as a system-level stability check. In general, this standard has been assembled with the supply-side and load-side requirements so that the EPS and loads can be developed separately. This criterion uses design data from both the supply and load as the ultimate overall stability check. The approach is based on the significant relationship between source and load impedance and the effect of this relationship on system stability. The stability criteria establish that maintaining a 3 decibel (dB) (0.707) impedance margin between unity gain and the ratio of source and load impedance provides system stability. When the margin for impedance magnitude is less than 3 dB, then the phase margin cannot enter the Forbidden Zone shown in Figure 3.3.1-1: Nyquist Stability Criteria, over the span of

frequencies from 30 hertz (Hz) to 100 kilohertz (kHz). The application of the stability criteria should consider all possible source and loads combinations that may occur, including the failure of any equipment connected to the bus. On the Nyquist plot, the phase margin is specified only at the crossover points where Z_S divided by Z_L intersects the unit circle. The stability criteria are discussed further in Section 0 of this document. Maintaining stability is especially important to maintaining power quality in a multiple load and multiple channel system because instability in any part of the system will cause degradation, if not a total loss, to the power quality delivered to any other part of the system.



NOTE:

1. Z_S is the output impedance of the source subsystem.
2. Z_L is the input impedance of the load subsystem.

FIGURE 3.3.1-1: NYQUIST STABILITY CRITERIA

3.3.1.6 ELECTROMAGNETIC COMPATIBILITY

PWR120-1007, PWR28-1007

An EPS EMI control plan shall be established in accordance with the vehicle mission requirements.

Rationale: Adopt a common EMI requirement for the power system.

3.3.2 120V EPS CHARACTERISTICS

3.3.2.1 NORMAL OPERATION

The electrical power system provides the following system power quality in the absence of failures or fault conditions.

3.3.2.1.1 STEADY STATE VOLTAGE

PWR120-1008

The EPS shall supply the steady-state voltage at the EPS/EPCE interface within the range of 98 to 136 VDC (120 VDC nominal) for load conditions from no-load to rated capacity of the system.

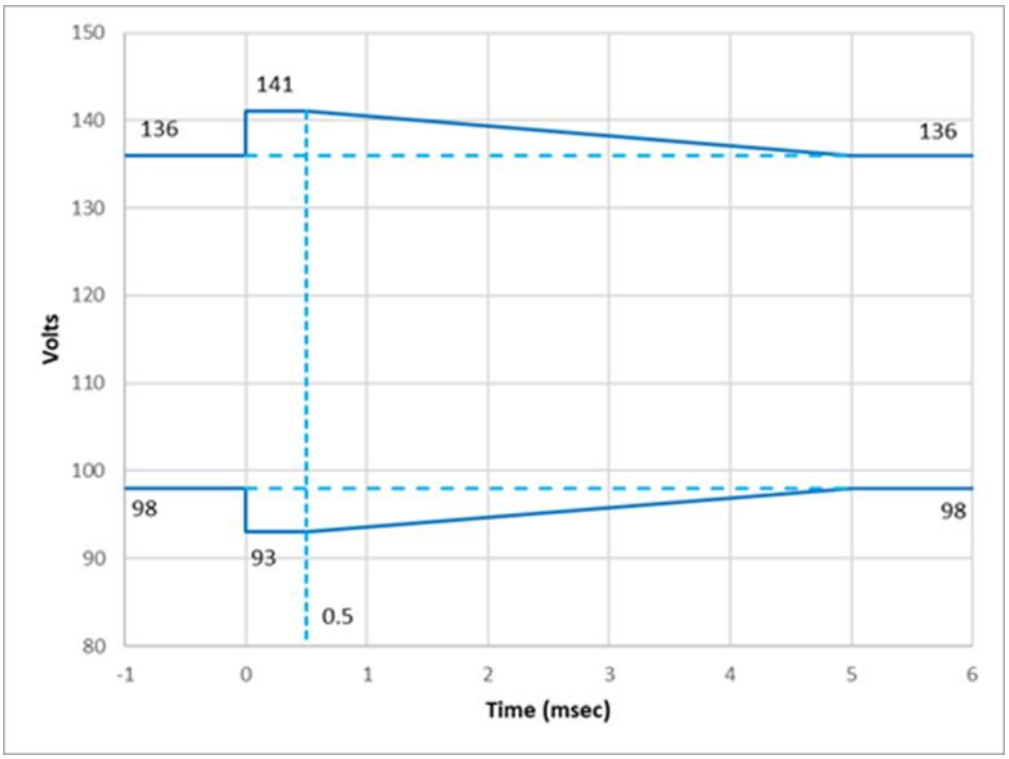
Rationale: Establish a system voltage range for the EPS at the input terminals of a load to account for the voltage drops throughout the EPS and stay within the prescribed nominal steady-state voltage. The voltage ranges include the expected voltage swing for a power system that is comprised of batteries and either solar arrays or fuel cell power generation with nominal voltage losses due to the EPS distribution system. It is important to note that this defines the generic EPS/EPCE load interface voltage, and that this standard assumes a nominal EPS/EPCE load interface voltage of 120 VDC. Other upper-tier EPS system interface voltages may be defined at other areas within the overall EPS system and require voltage performance margins to be added.

3.3.2.1.2 NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR120-1009

The electric power shall remain within the magnitude and duration limits for voltage transients shown in Figure 3.3.2-1: 120 VDC EPS Normal Transient Response.

Rationale: This requirement establishes a normal operating magnitude limit for voltage transients for an EPCE interface due to normal switching of loads that will provide sufficient operational voltage margin for the downstream EPCE. This power envelope may differ from the main power bus transient. Extreme high and low bus voltages are assumed contingency cases, and while experiencing these conditions it is assumed that the power system will experience small changes in load steps. It is important to note that this defines the generic EPS/EPCE load interface performance. Other upper-tier EPS system interfaces may be defined at other areas within the overall EPS system and require performance margins to be added.



NOTE: The envelope shown applies to the transient responses exclusive of any periodic noise components that may be present.

FIGURE 3.3.2-1: 120 VDC EPS NORMAL TRANSIENT RESPONSE

3.3.2.1.3 RIPPLE VOLTAGE

Ripple voltages are superimposed on the power system and can dramatically affect instrumentation and other sensitive loads. The ripple voltage is a primary power quality parameter. The total system ripple voltage is comprised of the collective contributions from sources and loads. Design-specific power specifications may allocate the ripple for the EPS itself at specified upper-tier EPS interfaces, including the generic EPS/EPCE interface. Ripple is defined by three characteristics; peak ripple voltage, ripple voltage amplitude, and ripple voltage spectrum.

3.3.2.1.3.1 PEAK RIPPLE VOLTAGE

PWR120-1010

The peak ripple voltage shall be less than 3.5 Volts peak (Vp) in a bandwidth of 30 Hz to 1 megahertz (MHz).

Rationale: Establish a worst-case peak system ripple voltage with the collective contributions from sources and loads. The requirement particularly targets ripple voltage contributions generated by pulses, doublet pulses, and spike waveforms.

3.3.2.1.3.2 RIPPLE VOLTAGE AMPLITUDE

PWR120-1011

The ripple voltage amplitude shall be less than 2.5 Volts root-mean-square (Vrms) in a bandwidth of 30 Hz to 1 MHz.

Rationale: Establish a worst-case maximum system ripple voltage as a primary power quality parameter. This requirement limits the total root-mean-square (rms) voltage composite of all ripple harmonics. The requirement particularly targets ripple voltage contributions generated by low frequency and non-harmonic loads.

3.3.2.1.3.3 RIPPLE VOLTAGE SPECTRUM

PWR120-1012

The frequency distribution of the ripple voltage shall remain within the limits shown in Figure 3.3.2-2: 120 VDC Ripple Voltage Spectral Components.

Rationale: Establish a worst-case system ripple voltage characterized against a frequency range with collective contributions from sources and loads. This system ripple spectrum defines power quality for the electromagnetic conducted emissions requirement. This spectrum requirement limits ripple voltage contribution generated by periodic waveforms such as sine, square, and triangle waves.

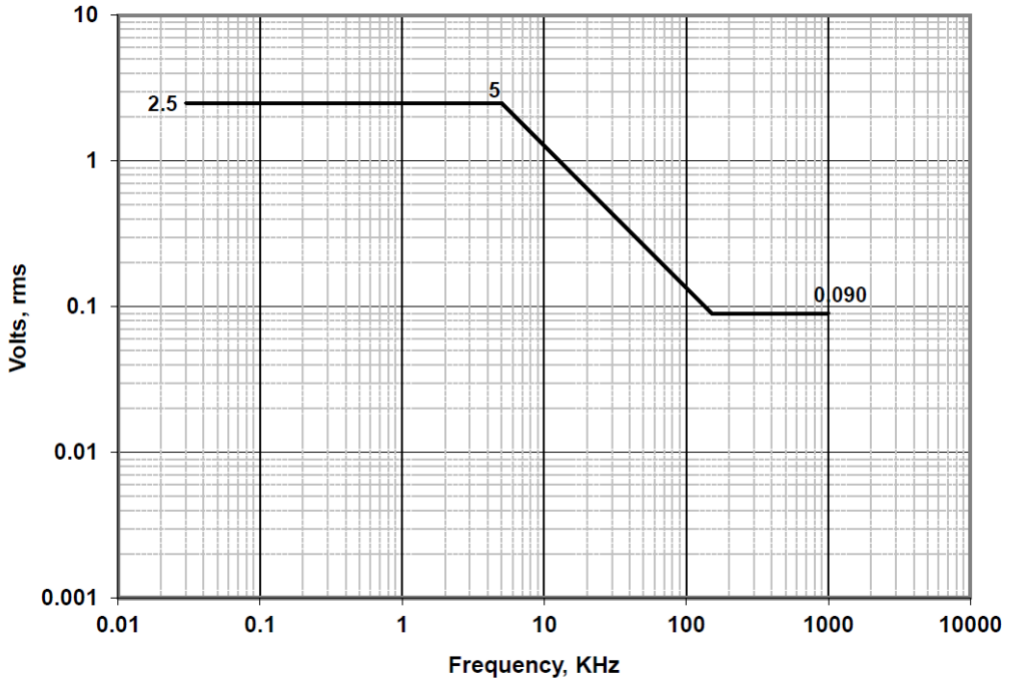


FIGURE 3.3.2-2: 120 VDC RIPPLE VOLTAGE SPECTRAL COMPONENTS

3.3.2.1.4 EXTERNAL POWER SOURCE

PWR120-1013

External electric power sources shall supply power having the characteristics as specified within this standard.

Rationale: External power (any auxiliary or emergency power) must maintain the same ripple, transient, stability, isolation, and fault coordination characteristics that the EPS maintains regardless of whether the external power is operating stand-alone or integrated with the power system.

3.3.2.1.5 INRUSH/SURGE CURRENT TRANSIENTS

PWR120-1014

The EPS shall support load inrush/surge currents of:

- 0.012 A*Sec / A for loads with currents 0A < I < 10A;
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A.

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000 microfarad (μF) for a 10 Amp source at 120 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 120 V = 1000μF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 120 V = 1000 μF.*

EPS designs may require additional power conditioning for a large inrush condition to limit the bus voltage drop.

3.3.2.2 ABNORMAL OPERATION

The electrical power system provides the following system power quality in the presence of failures or fault conditions.

3.3.2.2.1 ABNORMAL REVERSE CURRENT

PWR120-1015

The EPS shall accept reverse currents under abnormal conditions without damage.

- 0.012 A*Sec / A for loads with currents 0A < I < 10A
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000 microfarad (μF) for a 10 Amp source at 120 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 120 V = 1000μF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 120 V = 1000 μF.*

EPS designs may require additional power conditioning for a large inrush condition to limit the bus voltage drop.

3.3.2.2.2 EPS FAULT PROTECTION

PWR120-1016

The EPS power distribution system shall provide overcurrent protection to branch circuits that limit fault currents and isolate faults.

Rationale: The requirement establishes a consistent fault mitigation method for the EPS interface to the EPCE. Faults in any load branch must be cleared and not cause any other load to become disabled. The protection should limit/clear the overcurrent condition to maintain the EPS power quality. The fault and/or overcurrent protection should not trip off due to expected inrush/surge transients.

3.3.2.2.3 OVERVOLTAGE SURGE

PWR120-1017

The EPS source at the EPCE interface shall recover from an overvoltage surge due to an EPS fault condition to within power quality as shown in Figure 3.3.2-3: 120 VDC EPS Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: Establish a worst-case overvoltage condition at the EPCE interface during fault clearing from EPS failures. This condition is produced from stored energy within the power distribution system and loads. Power system designers need to select hardware to withstand anticipated worst-case overvoltage without damaging parts of the power system. It must be noted that this event is defined at the EPCE interface.

This condition is produced from stored energy within the power distribution system and loads. Power system designers need to select hardware to withstand anticipated worst-case overvoltage without damaging parts of the power system.

3.3.2.2.4 UNDERVOLTAGE SURGE

PWR120-1018

The EPS source shall recover from an undervoltage surge due to an EPS fault condition to within power quality as shown in Figure 3.3.2-3: 120 VDC EPS Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: Establish a worst-case undervoltage condition for the EPS at the EPCE interface, experienced from fault clearing. This condition depends on the location of the fault in the load distribution power system and where it is observed. Clearing of load faults generally will not induce conditions as severe and distribution switchgear that limits fault currents closer to the EPCE minimizes the effects of system faults. The undervoltage condition will fall outside the normal operating voltage, (as low as zero volts), clear the condition, reconfigure, and return to within power quality. Power quality will be re-established for users outside of the faulted area. Power system designers need to select hardware to withstand anticipated worst-case undervoltage conditions without damaging parts of the power system. This requirement does not intend to specify that any part of the power system will be required to operate through the transient event or should configure to operate immediately following the event. The intent is to establish that the source may be removed such that all of the downstream EPCE may cease operating and will not be damaged. Other considerations such as criticality or system operational modes need to be used to determine the recovery state. It must be noted that this event is defined at the EPCE interface.

Consider criticality or system operational modes when determining recovery state.

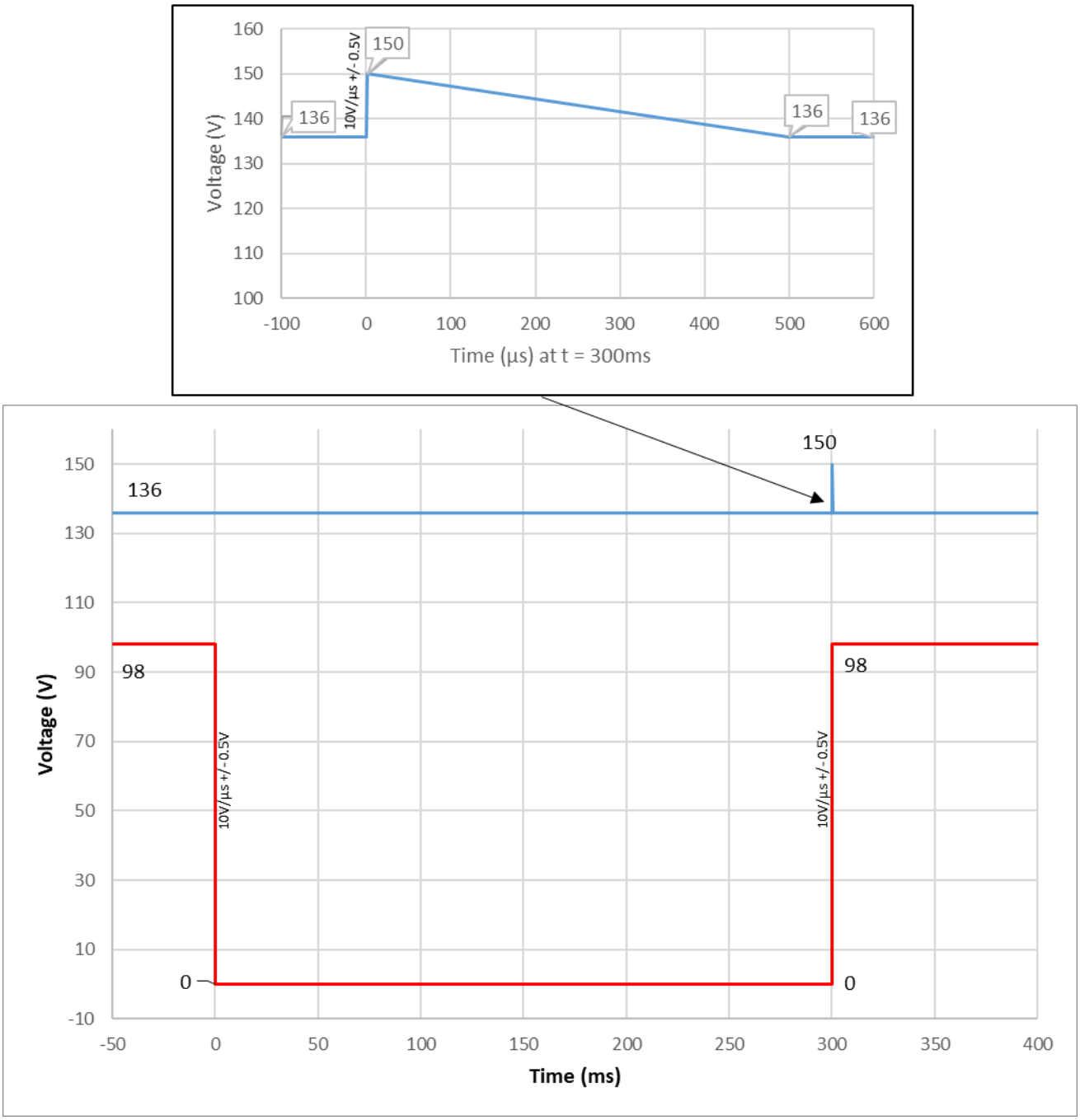


FIGURE 3.3.2-3: 120 VDC EPS ABNORMAL VOLTAGE LIMITS FOR OVERVOLTAGE AND UNDERVOLTAGE

3.3.2.2.5 EMERGENCY OPERATION

PWR120-1019

The EPS shall be capable of supplying power until all energy sources are depleted.

Rationale: The EPS should provide for contingency cases where the primary power generation source is disabled or unavailable to allow for 100% power system utilization. The intent is to force the power system to continue operation until it can no longer provide the minimum voltage as specified in this standard.

3.3.2.2.6 FAULTS

Abnormal conditions occur when a system malfunctions or a fault/failure of the EPS occurs. The protective devices of the EPS during this condition operate to isolate or remove the faulted system from the appropriate EPS interface and recover/reconfigure from the fault/failure. Under abnormal conditions, the power quality will not be maintained. Power system designs must take into account these major system fault conditions.

3.3.2.2.6.1 HIGH IMPEDANCE FAULTS

PWR120-1020

The EPS shall isolate high impedance faults (soft faults) for overcurrent conditions in excess of 150% of rated current of the upstream protective device for a maximum total clearing time less than 4 seconds (from time of detection).

Rationale: Establish a worst-case clearing time constraint for overcurrent conditions that stress the overall distribution system. The overcurrent conditions must be removed from the EPS. Clearing times for various loads will be based on mission requirements, criticality of the load, and switchgear requirements. The intent of this requirement is to constrain fault current conditions and not directly define the switchgear characteristics. These are upper bounds and projects can implement a protection schema which is faster than this. The fault and/or overcurrent protection should not trip off due to expected inrush/surge transients.

3.3.2.2.6.2 HIGH CURRENT FAULTS

PWR120-1021

The EPS shall isolate high current faults (short circuit) for overcurrent conditions in excess of 400% of the rated current of the upstream protective device with a maximum total clearing time less than or equal to 15 milliseconds (ms) (from time of detection).

Rationale: Establish a worst-case clearing time for high current faults (short circuit or a load resistance that produces equivalent 400% load current) type conditions that stress the distribution system. Short circuit conditions have to be removed quickly from the EPS before damaging other areas of the system. Faster clearing times under these conditions will be based on mission requirements, criticality of the loads, and switchgear requirements. The intent of this requirement is to constrain fault current conditions and not directly define the switchgear characteristics. The fault and/or overcurrent protection should not trip off due to expected inrush/surge transients.

3.3.2.2.6.3 EPS, FAULT CONTAINMENT

PWR120-1022

The EPS shall provide fault protection coordination so that the protective circuit closest to the fault will contain an electrical short circuit in the electrical distribution system.

Rationale: Establish fault coordination as fundamental in maintaining the operability of the power system while isolating failures and minimizing the impact of failures to the remaining power system at the EPS. Fault coordination across the interface is necessary to ensure that load branch faults will be cleared without affecting any other load. Coordination must take into account upstream protective equipment, stored energy causing damaging currents, and inrush currents during fault recovery. This coordination will also be implemented downstream from current limiting switchgear to isolate faults occurring in any of the power controller's output lines to contain the fault so the device closest to the fault trips first and power can continue to be provided to the remaining unfaulted outputs. Overcurrent protection should be located at the output of the distribution system. The overcurrent protection will isolate a particular branch feed from the power system. Select overcurrent devices based on the overall protection coordination.

3.3.3 28V EPS CHARACTERISTICS

3.3.3.1 NORMAL OPERATION

The electrical power system provides the following system power quality in the absence of failures or fault conditions.

3.3.3.1.1 STEADY STATE VOLTAGE

PWR28-1008

The EPS shall supply the steady-state voltage at the EPS/EPCE interface within the range of 23 to 36 VDC (28 VDC nominal) for load conditions from no-load to the rated capacity of the system.

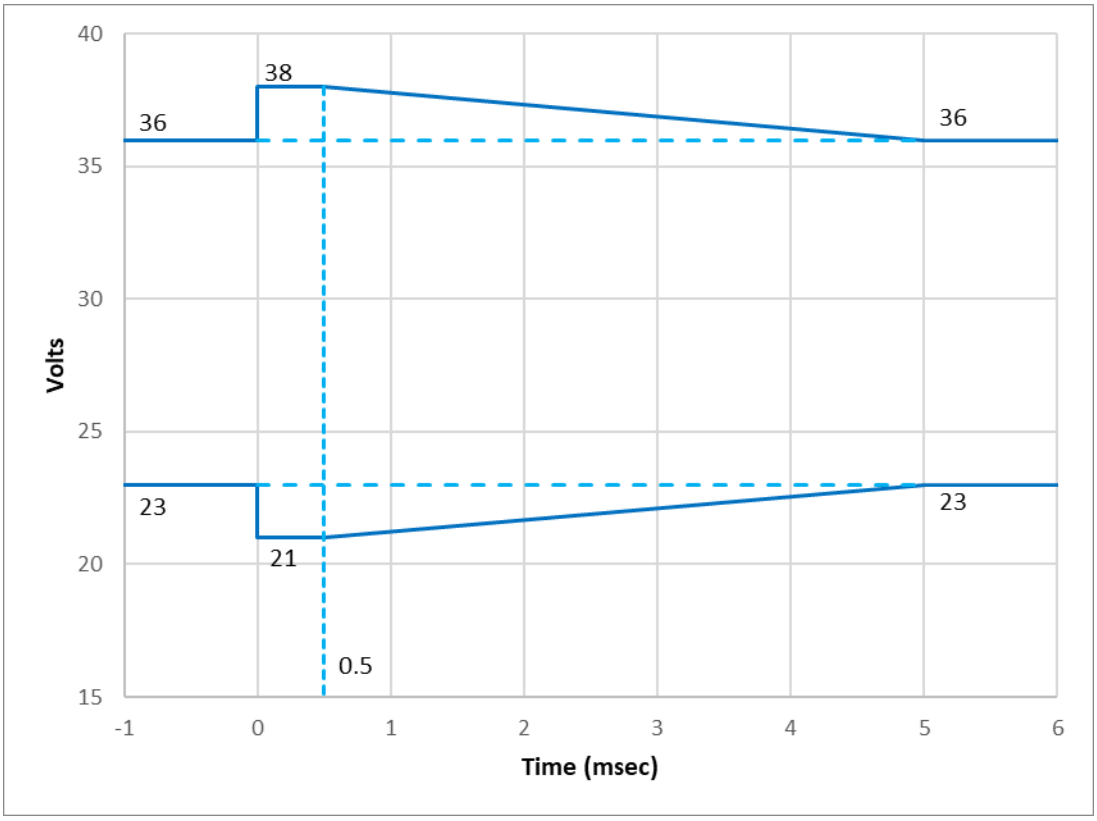
Rationale: Establish a system voltage range for the EPS at the input terminals of a load to account for the voltage drops throughout the EPS and stay within the prescribed nominal steady-state voltage. The voltage ranges include the expected voltage swing for a power system that is comprised of batteries and either solar arrays or fuel cell power generation with nominal voltage losses due to the EPS distribution system. It is important to note that this defines the generic EPS/EPCE load interface voltage, and that this standard assumes a nominal EPS/EPCE load interface voltage of 28 VDC. Other upper-tier EPS system interface voltages may be defined at other areas within the overall EPS system and require voltage performance margins to be added.

3.3.3.1.2 NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR28-1009

The electric power shall remain within the magnitude and duration limits for voltage transients shown in Figure 3.3.3-1: 28 VDC EPS Normal Transient Response.

Rationale: This requirement establishes a normal operating magnitude limit for voltage transients for an EPCE interface due to normal switching of loads that will provide sufficient operational voltage margin for the downstream EPCE. This power envelope may differ from the main power bus transient. Extreme high and low bus voltages are assumed contingency cases, and while experiencing these conditions it is assumed that the power system will experience small changes in load steps. It is important to note that this defines the generic EPS/EPCE load interface performance. Other upper-tier EPS system interfaces may be defined at other areas within the overall EPS system and require performance margins to be added.



NOTE: The envelope shown applies to the transient responses exclusive of any periodic noise components that may be present.

FIGURE 3.3.3-1: 28 VDC EPS NORMAL TRANSIENT RESPONSE

3.3.3.1.3 RIPPLE VOLTAGE

Ripple voltages are superimposed on the power system and can dramatically affect instrumentation and other sensitive loads. The ripple voltage is a primary power quality parameter. The total system ripple voltage is comprised of the collective contributions from sources and loads. Design-specific power specifications may allocate the ripple for the EPS itself at specified upper-tier EPS interfaces, including the generic EPS/EPCE

interface. Ripple is defined by three characteristics; peak ripple voltage, ripple voltage amplitude, and ripple voltage spectrum.

3.3.3.1.3.1 PEAK RIPPLE VOLTAGE

PWR28-1010

The peak ripple voltage shall be less than 1.5 Volts peak (Vp) in a bandwidth of 30 Hz to 1 MHz.

Rationale: Establish a worst-case peak system ripple voltage with the collective contributions from sources and loads. The requirement particularly targets ripple voltage contributions generated by pulses, doublet pulses, and spike waveforms.

3.3.3.1.3.2 RIPPLE VOLTAGE AMPLITUDE

PWR28-1011

The ripple voltage amplitude shall be less than 1.0 Volts root-mean-square (Vrms) in a bandwidth of 30 Hz to 1 MHz.

Rationale: Establish a worst-case maximum system ripple voltage as a primary power quality parameter. This requirement limits the total root-mean-square (rms) voltage composite of all ripple harmonics. The requirement particularly targets ripple voltage contributions generated by low frequency and non-harmonic loads.

3.3.3.1.3.3 RIPPLE VOLTAGE SPECTRUM

PWR28-1012

The frequency distribution of the ripple voltage shall remain within the limits shown in Figure 3.3.3-2: 28 VDC Ripple Voltage Spectral Components.

Rationale: Establish a worst-case system ripple voltage characterized against a frequency range with collective contributions from sources and loads. This system ripple spectrum defines power quality for the electromagnetic conducted emissions requirement. This spectrum requirement limits ripple voltage contribution generated by periodic waveforms such as sine, square, and triangle waves.

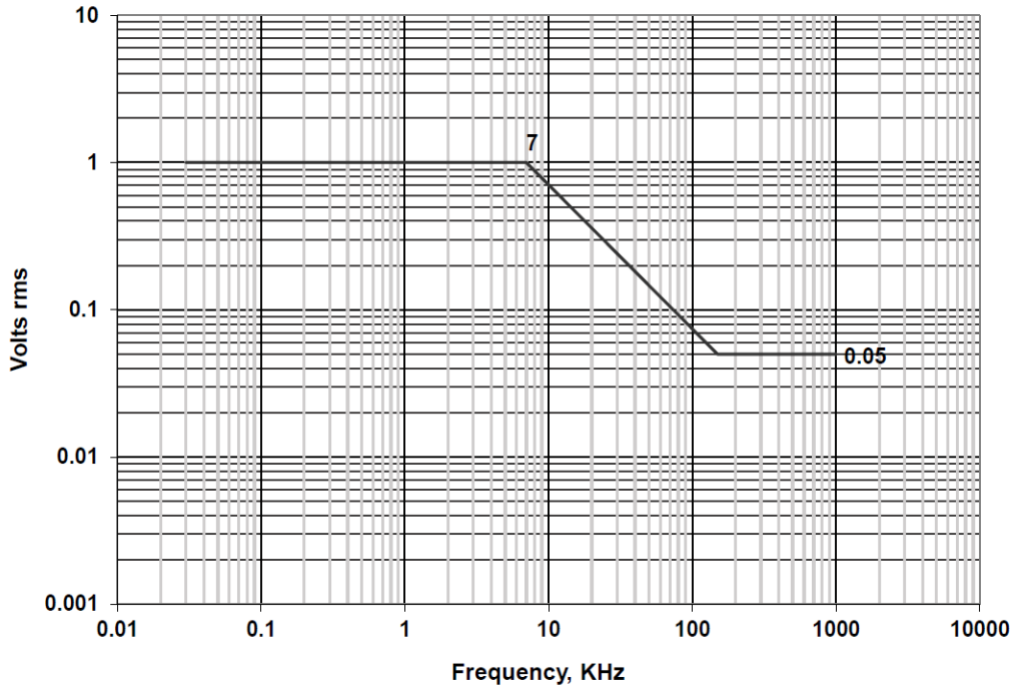


FIGURE 3.3.3-2: 28 VDC RIPPLE VOLTAGE SPECTRAL COMPONENTS

3.3.3.1.4 EXTERNAL POWER SOURCE

PWR28-1013

External electric power sources shall supply power having the characteristics as specified within this standard.

Rationale: External power (any auxiliary or emergency power) must maintain the same ripple, transient, stability, isolation, and fault coordination characteristics that the EPS maintains regardless of whether the external power is operating stand-alone or integrated with the power system.

3.3.3.1.5 INRUSH/SURGE CURRENT TRANSIENTS

PWR28-1014

The EPS shall support load inrush/surge currents of:

- 0.012 A*Sec / A for loads with currents 0A < I < 10A;
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A.

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a

margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 4286 microfarad (µF) for a 10 Amp source at 28 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 28 V = 4286µF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 28 V = 4286 µF.*

EPS designs may require additional power conditioning for a large inrush condition to limit the bus voltage drop.

3.3.3.2 ABNORMAL OPERATION

The electrical power system provides the following system power quality in the presence of failures or fault conditions.

3.3.3.2.1 ABNORMAL REVERSE CURRENT

PWR28-1015

The EPS shall accept reverse currents under abnormal conditions without damage.

- 0.012 A*Sec / A for loads with currents 0A < I < 10A
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 4286 microfarad (µF) for a 10 Amp source at 28 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 28 V = 4286µF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 28 V = 4286 µF.*

EPS designs may require additional power conditioning for a large inrush condition to limit the bus voltage drop.

3.3.3.2.2 EPS FAULT PROTECTION

PWR28-1016

The EPS power distribution system shall provide overcurrent protection to branch circuits that limit fault currents and isolate faults.

Rationale: The requirement establishes a consistent fault mitigation method for the EPS interface to the EPCE. Faults in any load branch must be cleared and not cause any other load to become disabled. The protection should limit/clear the overcurrent condition to maintain the EPS power quality. The fault and/or overcurrent protection should not trip off due to expected inrush/surge transients.

3.3.3.2.3 OVERVOLTAGE SURGE

PWR28-1017

The EPS source at the EPCE interface shall recover from an overvoltage surge due to an EPS fault condition to within power quality as shown in Figure 3.3.3-3: 28 VDC EPS Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: Establish a worst-case overvoltage condition at the EPCE interface during fault clearing from EPS failures. This condition is produced from stored energy within the power distribution system and loads. Power system designers need to select hardware to withstand anticipated worst-case overvoltage without damaging parts of the power system. It must be noted that this event is defined at the EPCE interface.

3.3.3.2.4 UNDERVOLTAGE SURGE

PWR28-1018

The EPS source shall recover from an undervoltage surge due to an EPS fault condition to within power quality as shown in Figure 3.3.3-3: 28 VDC EPS Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: Establish a worst-case undervoltage condition for the EPS at the EPCE interface, experienced from fault clearing. This condition depends on the location of the fault in the load distribution power system and where it is observed. Clearing of load faults generally will not induce conditions as severe and distribution switchgear that limits fault currents closer to the EPCE minimizes the effects of system faults. The undervoltage condition will fall outside the normal operating voltage, (as low as zero volts), clear the condition, reconfigure, and return to within power quality. Power quality will be re-established for users outside of the faulted area. Power system designers need to select hardware to withstand anticipated worst-case undervoltage conditions without damaging parts of the power system. This requirement does not intend to specify that any part of the power system will be required to operate through the transient event or should configure to operate immediately following the event. The intent is to establish that the source may be removed such that all of the downstream EPCE may cease operating and will not be damaged. Other considerations such as criticality or system operational modes need to be used to determine the recovery state. It must be noted that this event is defined at the EPCE interface.

Consider criticality or system operational modes when determining recovery state.

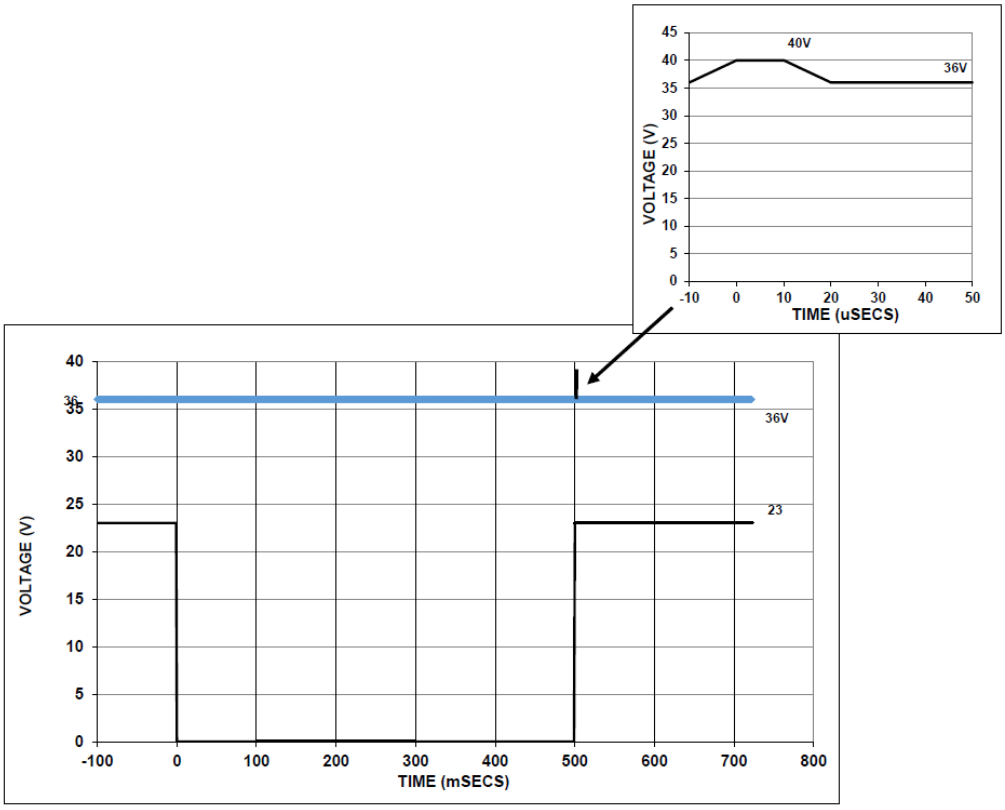


FIGURE 3.3.3-3: 28 VDC EPS ABNORMAL VOLTAGE LIMITS FOR OVERVOLTAGE AND UNDERVOLTAGE

3.3.3.2.5 EMERGENCY OPERATION

PWR28-1019

The EPS shall be capable of supplying power until all energy sources are depleted.

Rationale: The EPS should provide for contingency cases where the primary power generation source is disabled or unavailable to allow for 100% power system utilization. The intent is to force the power system to continue operation until it can no longer provide the minimum voltage as specified in this standard.

3.3.3.2.6 FAULTS

Abnormal conditions occur when a system malfunctions or a fault/failure of the EPS occurs. The protective devices of the EPS during this condition operate to isolate or remove the faulted system from the appropriate EPS interface and recover/reconfigure from the fault/failure. Under abnormal conditions, the power quality will not be maintained. Power system designs must take into account these major system fault conditions.

3.3.3.2.6.1 HIGH IMPEDANCE FAULTS

PWR28-1020

The EPS shall isolate high impedance faults (soft faults) for overcurrent conditions in excess of 150% of rated current of the upstream protective device for a maximum total clearing time less than 4 seconds (from time of detection).

Rationale: Establish a worst-case clearing time constraint for overcurrent conditions that stress the overall distribution system. The overcurrent conditions must be removed from the EPS. Clearing times for various loads will be based on mission requirements, criticality of the load, and switchgear requirements. The intent of this requirement is to constrain fault current conditions and not directly define the switchgear characteristics. These are upper bounds and projects can implement a protection schema which is faster than this. The fault and/or overcurrent protection should not trip off due to expected inrush/surge transients.

3.3.3.2.6.2 HIGH CURRENT FAULTS

PWR28-1021

The EPS shall isolate high current faults (short circuit) for overcurrent conditions in excess of 400% of the rated current of the upstream protective device with a maximum total clearing time less than or equal to 15 milliseconds (ms) (from time of detection).

Rationale: Establish a worst-case clearing time for high current faults (short circuit or a load resistance that produces equivalent 400% load current) type conditions that stress the distribution system. Short circuit conditions have to be removed quickly from the EPS before damaging other areas of the system. Faster clearing times under these conditions will be based on mission requirements, criticality of the loads, and switchgear requirements. The intent of this requirement is to constrain fault current conditions and not directly define the switchgear characteristics. The fault and/or overcurrent protection should not trip off due to expected inrush/surge transients.

3.3.3.2.6.3 EPS, FAULT CONTAINMENT

PWR28-1022

The EPS shall provide fault protection coordination so that the protective circuit closest to the fault will contain an electrical short circuit in the electrical distribution system.

Rationale: Establish fault coordination as fundamental in maintaining the operability of the power system while isolating failures and minimizing the impact of failures to the remaining power system at the EPS. Fault coordination across the interface is necessary to ensure that load branch faults will be cleared without affecting any other load. Coordination must take into account upstream protective equipment, stored energy causing damaging currents, and inrush currents during fault recovery. This coordination will also be implemented downstream from current limiting switchgear to isolate faults occurring in any of the power controller's output lines to contain the fault so

the device closest to the fault trips first and power can continue to be provided to the remaining unfaulted outputs. Overcurrent protection should be located at the output of the distribution system. The overcurrent protection will isolate a particular branch feed from the power system. Select overcurrent devices based on the overall protection coordination.

3.4 ELECTRICAL POWER CONSUMING EQUIPMENT INTERFACE PERFORMANCE

The following requirements are imposed on each electric power load to guarantee the required EPS power quality is maintained. The electrical power characteristics specified herein are minimum requirements for EPCE electrical loads. An EPCE constitutes every fixed or portable device that consumes electric power. The following paragraphs describe the requirements on electrical users. The performance is specified at the input terminals of individual EPCE (electrical loads).

The requirements following a PWR120-XXXX label pertain to a 120V system and the requirements following a PWR28-XXXX label pertain to a 28V system.

3.4.1 120V EPCE CHARACTERISTICS

3.4.1.1 NORMAL OPERATION

The following requirements cover normal operations of the EPCE in the absence of failures or fault conditions.

3.4.1.1.1 STEADY STATE OPERATION

PWR120-2001

EPCE shall operate with an input voltage within the range of 98 to 136 VDC.

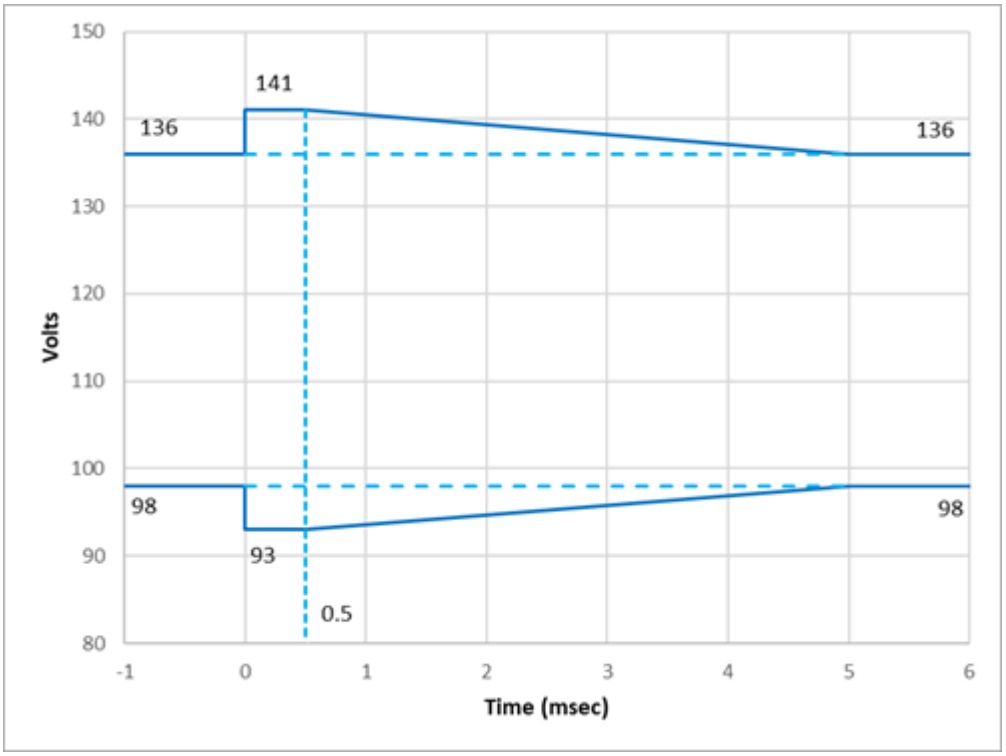
Rationale: This voltage is defined at the input terminals of the EPCE. The EPCE are designed to operate within the full range of the voltage parameter to allow voltage compatibility across multiple interfaces as discussed in paragraph 3.2.

3.4.1.1.2 EPCE POWER INTERFACE, NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR120-2002

The EPCE shall operate within the EPS system voltage transient limits defined in Figure 3.4.1-1: 120 VDC EPCE Normal Transient Response.

Rationale: Figure 3.4.1-1: 120 VDC EPCE Normal Transient Response, shows the normal operating magnitude and duration limits for voltage transients at the EPCE power interface due to normal switching of loads. The transient range does not take into account any margins that system designers need to take into account in the load design. The extreme high and low bus voltages are assumed contingency cases and while experiencing these conditions it is assumed that the power system will experience small changes in load steps. This power envelop may differ from the main power bus transient. The EPCE must operate nominally anywhere within the upper and lower boundary condition.



Note: The envelope shown applies to the transient responses exclusive of any periodic noise components that may be present.

FIGURE 3.4.1-1: 120 VDC EPCE NORMAL TRANSIENT RESPONSE

3.4.1.1.3 EPCE RIPPLE COMPATIBILITY

EPCE may potentially emit or conduct excessive electrical noise (e.g., due to internal switching frequencies of a converter), and this noise (ripple voltages and currents) can dramatically affect instrumentation and other sensitive loads. Likewise, the performance of an EPCE may be adversely affected by noise produced by other devices connected to the power distribution system. As a result, the EPCE emissions and performance in the presence of system ripple will be set.

3.4.1.1.3.1 EPCE, RIPPLE EMISSIONS

PWR120-2003

EPCE shall meet the emissions limits as set by the EMI control plan.

Rationale: Ripple currents and voltages superimposed on the 120 VDC system can have dramatic effects on instrumentation and other sensitive loads. The total system conducted ripple voltage is the collective contributions from sources and loads. EPCE must minimize ripple contribution to the system.

3.4.1.1.3.2 EPCE, RIPPLE VOLTAGE SPECTRUM

PWR120-2004

EPCE shall operate nominally and maintain stability when subjected to the ripple spectrum as specified in the EMI control plan.

Rationale: Ripple voltage is characterized against frequency range and describes the worst-case ripple voltages with collective contributions from sources and loads. This system ripple spectrum is a basic power quality requirement, as defined by the EMI Control Plan, and is the basis for the electromagnetic susceptibility requirements. Ripple voltages are shown as a maximum, which include the system ripple voltage and the EPCE ripple voltage introduced by a load. The system ripple voltage does not take into account any margins that system designers need to apply to the load design. This spectrum susceptibility requirement encompasses the ripple voltage contribution generated by periodic waveforms such as sine, square, and triangle waves.

3.4.1.1.4 LOCAL STABILITY

Local stability refers to the stability of a load with respect to a representative source (not necessarily the EPS). Meeting the requirements of the following sections assures a margin of stability for the loads. Stability is essential to maintain power quality for system loads. These requirements need to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same power domain.

3.4.1.1.4.1 LARGE SIGNAL STABILITY

PWR120-2005

The EPCE shall provide a transient response that is damped as shown in Figure 3.4.1-2: Large Signal Stability Transient Response, when subjected to short-duration source-side transient voltages as defined in [PWR120-2005V] Figure 4.2.1-3: Large Signal Stability Test Transient.

Rationale: The transient response must decay and remain below 10 percent of the maximum response amplitude within 1.0 milliseconds as illustrated in Figure 3.4.1-2: Large Signal Stability Transient Response. The time to damp to 10 percent, as shown, is also referred to as settling time.

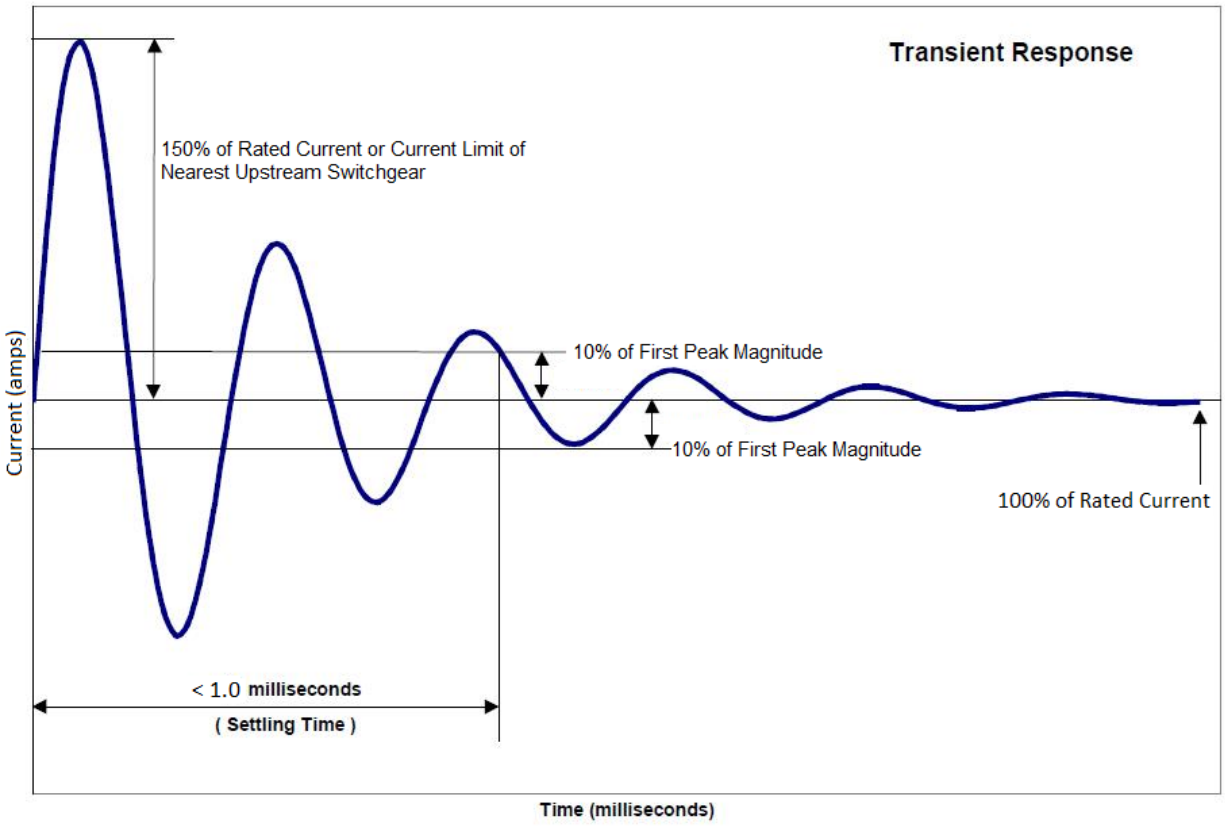


FIGURE 3.4.1-2: LARGE SIGNAL STABILITY TRANSIENT RESPONSE

3.4.1.1.4.2 EPCE INPUT IMPEDANCE

PWR120-2006

The EPCE input load impedance at the EPCE interface terminals shall be measured.

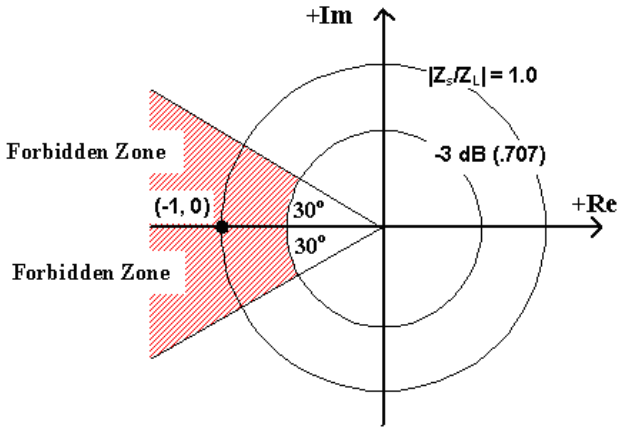
Rationale: The EPCE impedance value is required to calculate the stability margin of the source/load combination at the user input terminals. This document addresses a generic interface where the EPS and the EPCE have one common interface.

3.4.1.1.4.3 SMALL SIGNAL STABILITY

PWR120-2007

The EPCE shall maintain a complex impedance ratio of source impedance divided by load impedance (derived from [PWR120-1005] section 3.3.1.5.2) that remains outside the hatched area (Forbidden Zone) shown in Figure 3.4.1-3: Nyquist Stability Criteria, from 30 Hz to 100 kHz for all defined EPCE interfaces.

Rationale: The EPCE should meet this system-level requirement for small signal stability for all defined EPCE interfaces to maximize compatibility.



NOTE:

1. Z_S is the output impedance of the source subsystem.
2. Z_L is the input impedance of the load subsystem.

FIGURE 3.4.1-3: NYQUIST STABILITY CRITERIA

3.4.1.1.5 STARTUP AND INRUSH

3.4.1.1.5.1 CURRENT LIMITING SWITCHGEAR COMPATIBILITY

PWR120-2008

The EPCE shall be capable of operating from current limiting switchgear.

Rationale: Switchgear may limit the maximum input current to a value near the channel rating. EPCE with large values of energy storage (in capacitive filters or equivalent) will extend the rise time of the applied voltage as these filters charge. In extreme cases, the charging time may be greater than 100 ms. The EPCE must be compatible with this slow rise time. The EPCE should also try to minimize the amount of inrush/surge current seen by the switchgear.

3.4.1.1.5.2 INRUSH/SURGE CURRENT TRANSIENTS

PWR120-2009

The EPCE shall limit inrush/surge current to:

- 0.012 A*Sec / A for loads with currents 0A < I < 10A,
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a

margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000 microfarad (µF) for a 10 Amp source at 120 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 120 V = 1000µF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 120 V = 1000 µF.*

3.4.1.1.6 REVERSE CURRENT

PWR120-2010

The EPCE shall prevent reverse current flow back into the EPS source under normal operation for a fixed interface voltage.

Rationale: EPCE need to be designed to prevent current to out-flow into the power system under normal load operation with the voltage remaining constant. Loads, mainly motors and other inertial loads need to be designed as to not normally supply reverse currents (re-gen) into the distribution system and potentially raise the bus voltage to unacceptable levels causing the unintended tripping from other devices within the system. This requirement assumes a fixed steady state EPS bus voltage without any EPS droop in voltage therefore it is assumed that energy storage devices such as capacitors will not be affected by this requirement.

3.4.1.1.7 EPCE INPUT ISOLATION

PWR120-2011

The EPCE shall provide a minimum of 1 MΩ DC-resistive input isolation between each independent source input and between each source input and chassis.

Rationale: Maintain a consistent level of input isolation for EPCE and maintain isolation between power inputs such that no single failure within the EPCE will cause loss of electrical isolation between independent power buses or to chassis ground. These requirements apply to both supply and return circuits. Return isolation needs to be maintained when there are multiple circuits so as to not create a loop path (antenna), multiple return path (currents flowing through the single-point ground), or common mode currents. Isolation from chassis must be maintained to prevent currents through vehicle structure. Each EPCE must meet the failure requirements of the vehicle and should not cause loss of isolation between independent power busses.

3.4.1.2 ABNORMAL OPERATION

The EPCE is to return to normal operations after experiencing abnormal transients due to fault clearing identified in the following paragraphs. Abnormal transients occur when a malfunction or fault/failure is present in the system. The protective devices of the EPS,

during this condition, operate to isolate or remove the fault from the appropriate EPS interface and recover from the fault/failure.

3.4.1.2.1 ABNORMAL REVERSE CURRENTS

PWR120-2012

The EPCE shall limit reverse currents under abnormal conditions to:

- 0.012 A*Sec / A for loads with currents 0A < I < 10A;
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A.

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000 microfarad (μF) for a 10 Amp source at 120 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 120 V = 1000μF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 120 V = 1000 μF.*

3.4.1.2.2 OVERVOLTAGE SURGE

PWR120-2013

The EPCE shall meet the operational performance requirements as defined by the EPCE controlling documents after experiencing an overvoltage due to an EPS fault as shown in Figure 3.4.1-4: 120 VDC EPCE Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: This defines a worst-case overvoltage condition during fault clearing for major EPS faults. The user should not expect power quality during a fault condition. EPCE designers must take into account these conditions in the design of loads. EPCE designers need to select hardware to withstand anticipated worst-case overvoltage without permanently damaging system loads. EPCE controlling documents define how the equipment will operate nominally through the transient or recover to a safe state either automatically or by manual restart.

3.4.1.2.3 UNDERVOLTAGE SURGE

PWR120-2014

The EPCE shall meet the operational performance requirements as defined by the EPCE controlling documents after experiencing undervoltage due to an EPS fault as shown in Figure 3.4.1-4: 120 VDC EPCE Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: This event is defined at the EPCE interface. The user should not expect power quality during an EPS fault condition. The worst-case undervoltage condition will be outside of power quality while the system detects the fault, clears the condition, and re-establishes power to within power quality. Power quality will be re-established for users outside of the faulted area. EPCE controlling documents define how the equipment will operate nominally through the transient or recover to a safe state either automatically or by manual restart. The intent of this requirement is that loads should not be damaged or cause an unsafe condition as a result of undervoltage events. This requirement does not intend to stipulate whether any given load will be required to operate through the transient event or should configure to operate immediately following the event. The intent is to establish that the source may be removed such that all of the downstream EPCE may cease operating and will not be damaged. The EPCE input filter is not required to act as an uninterruptable power supply and any critical EPCE should have redundancy or multiple independent source inputs. Other considerations such as load criticality or system operational mode need to be used to determine recovery state. The EPCE can experience abnormal voltage droop and voltage overshoot greater than specified by the EPS, Normal Load Step Transient Voltage [PWR120-1009], section 3.3.2.1.2, while sharing an EPS source interface feeder with other loads. The magnitude of the abnormal voltage will be dependent on the loads applied and being applied/removed. Determination of the effects from the switching disturbances will be identified by the specific hardware controlling documents. It must be noted that this event is defined at the EPCE interface.

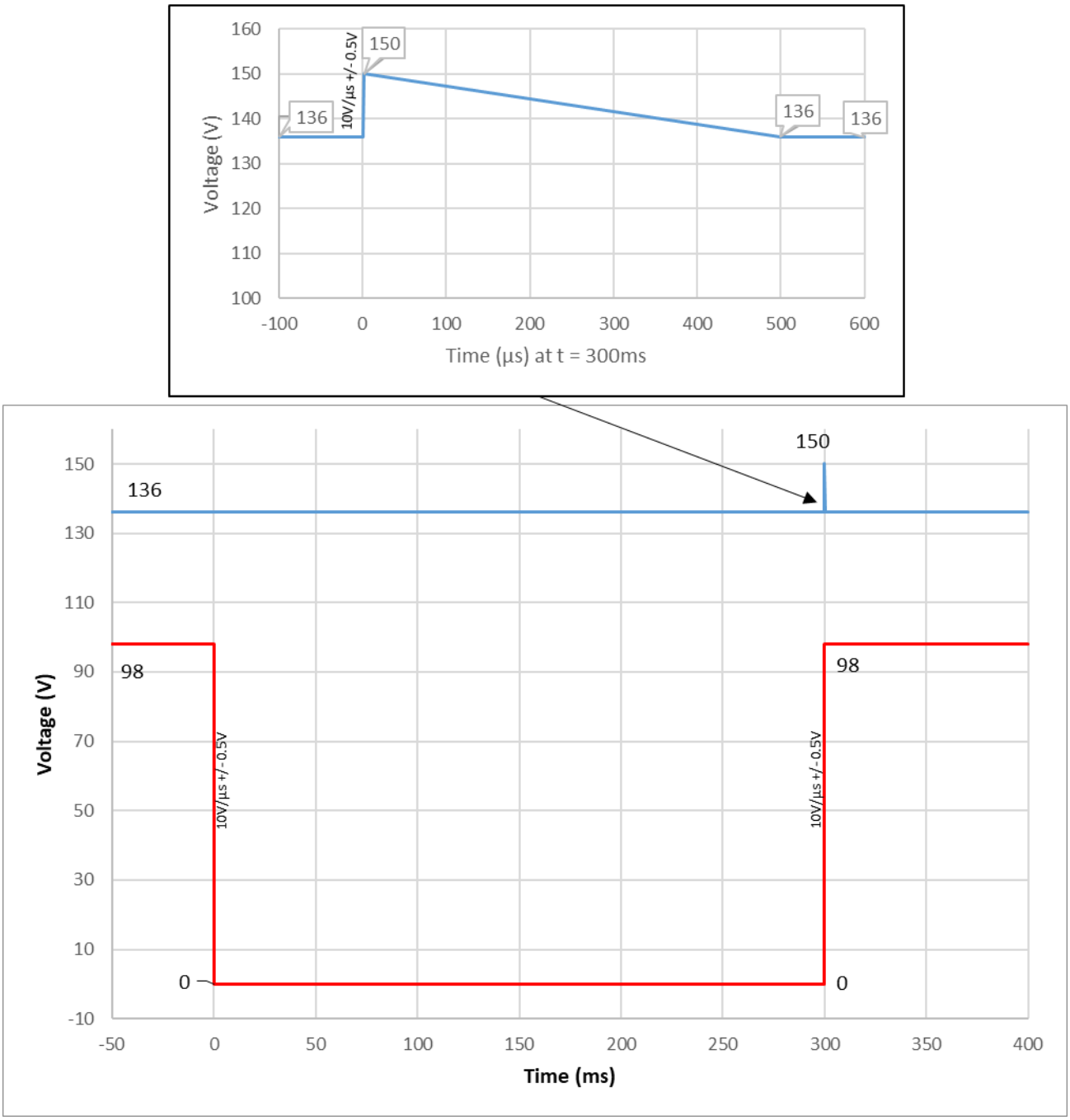


FIGURE 3.4.1-4: 120 VDC EPCE ABNORMAL VOLTAGE LIMITS FOR OVERVOLTAGE AND UNDERVOLTAGE

3.4.1.2.4 EMERGENCY OPERATION

PWR120-2015

EPCE deemed essential (contingency operations) shall continue to operate without loss of performance down to the reduced emergency voltage limit of 95 VDC.

Rationale: Establish an emergency operation system voltage range. The voltage allows for contingency cases where the primary power generation source is disabled or unavailable to allow for 100% power system utilization. This requirement typically applies to unregulated sources (i.e., battery) where there are a few specified EPCE that are required to continue to operate below normal minimum voltages for contingency operations. Operations below this contingency voltage is usually not practical due to the source no longer able to supply the required current for the EPCE to operate. This requirement shall be tailored to account for system specific characteristics such as voltage drop and voltage droop.

3.4.2 28V EPCE CHARACTERISTICS

3.4.2.1 NORMAL OPERATION

The following requirements cover normal operations of the EPCE in the absence of failures or fault conditions.

3.4.2.1.1 STEADY STATE OPERATION

PWR28-2001

EPCE shall operate with an input voltage within the range of 23 to 36 VDC.

Rationale: This voltage is defined at the input terminals of the EPCE. The EPCE are designed to operate within the full range of the voltage parameter to allow voltage compatibility across multiple interfaces as discussed in paragraph 3.2.

3.4.2.1.2 EPCE POWER INTERFACE, NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR28-2002

The EPCE shall operate within the EPS system voltage transient limits defined in Figure 3.4.2-1: 28 VDC EPCE Normal Transient Response.

Rationale: Figure 3.4.2-1 shows the normal operating magnitude and duration limits for voltage transients at the EPCE power interface due to normal switching of loads. The transient range does not take into account any margins that system designers need to take into account in the load design. The extreme high and low bus voltages are assumed contingency cases and while experiencing these conditions it is assumed that the power system will experience small changes in load steps. This power envelop may differ from the main power bus transient. The EPCE must operate nominally anywhere within the upper and lower boundary condition.

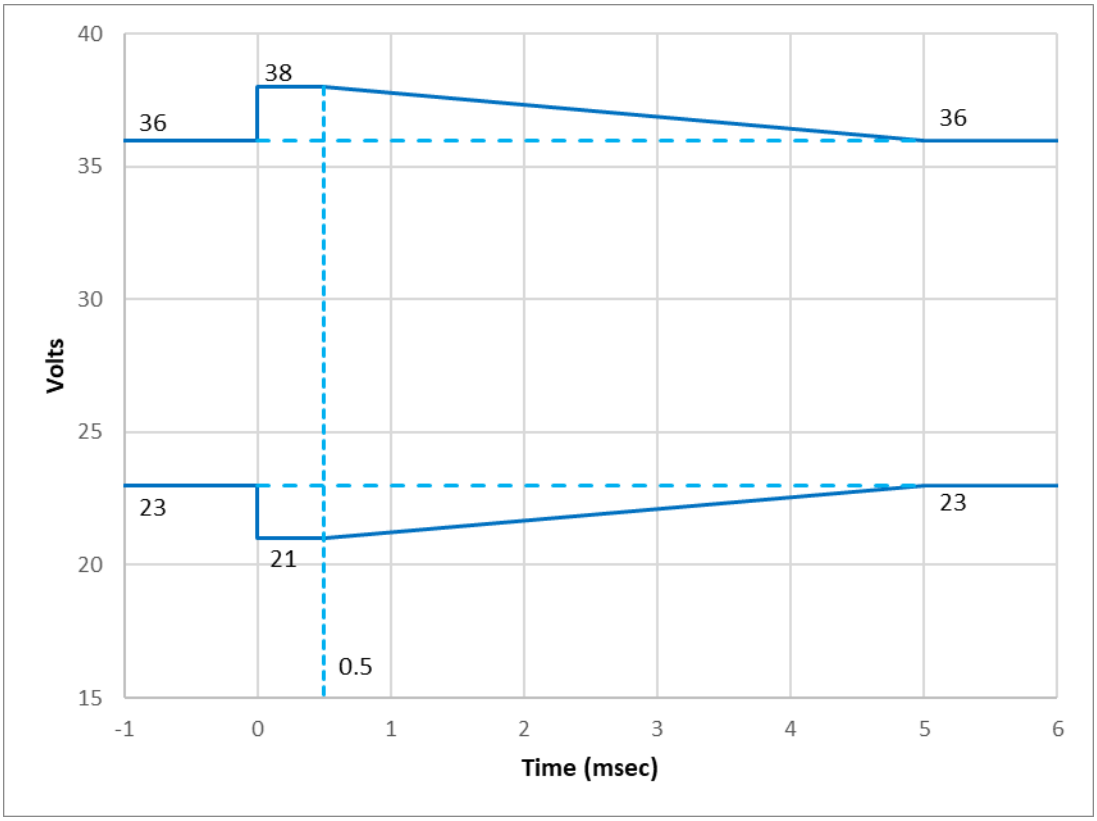


FIGURE 3.4.2-1: 28 VDC EPCE NORMAL TRANSIENT RESPONSE

3.4.2.1.3 EPCE RIPPLE COMPATIBILITY

EPCE may potentially emit or conduct excessive electrical noise (e.g., due to internal switching frequencies of a converter), and this noise (ripple voltages and currents) can dramatically affect instrumentation and other sensitive loads. Likewise, the performance of an EPCE may be adversely affected by noise produced by other devices connected to the power distribution system. As a result, the EPCE emissions and performance in the presence of system ripple will be set.

3.4.2.1.3.1 EPCE, RIPPLE EMISSIONS

PWR28-2003

EPCE shall meet the emissions limits as set by the EMI control plan.

Rationale: Ripple currents and voltages superimposed on the 28 VDC system can have dramatic effects on instrumentation and other sensitive loads. The total system conducted ripple voltage is the collective contributions from sources and loads. EPCE must minimize ripple contribution to the system.

3.4.2.1.3.2 EPCE, RIPPLE VOLTAGE SPECTRUM

PWR28-2004

EPCE shall operate nominally and maintain stability when subjected to the ripple spectrum as specified in the EMI control plan.

Rationale: Ripple voltage is characterized against frequency range and describes the worst-case ripple voltages with collective contributions from sources and loads. This system ripple spectrum is a basic power quality requirement, as defined by the EMI Control Plan, and is the basis for the electromagnetic susceptibility requirements. Ripple voltages are shown as a maximum, which include the system ripple voltage and the EPCE ripple voltage introduced by a load. The system ripple voltage does not take into account any margins that system designers need to apply to the load design. This spectrum susceptibility requirement encompasses the ripple voltage contribution generated by periodic waveforms such as sine, square, and triangle waves.

3.4.2.1.4 LOCAL STABILITY

Local stability refers to the stability of a load with respect to a representative source (not necessarily the EPS). Meeting the requirements of the following sections assures a margin of stability for the loads. Stability is essential to maintain power quality for system loads. These requirements need to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same power domain.

3.4.2.1.4.1 LARGE SIGNAL STABILITY

PWR28-2005

The EPCE shall provide a transient response that is damped as shown in Figure 3.4.2-2: Large Signal Stability Transient Response, when subjected to short-duration source-side transient voltages as defined in [PWR28-2005V] Figure 4.2.2-3: Large Signal Stability Test Transient.

Rationale: The transient response must decay and remain below 10 percent of the maximum response amplitude within 1.0 milliseconds as illustrated in Figure 3.4.2-2: Large Signal Stability Transient Response. The time to damp to 10 percent, as shown, is also referred to as settling time.

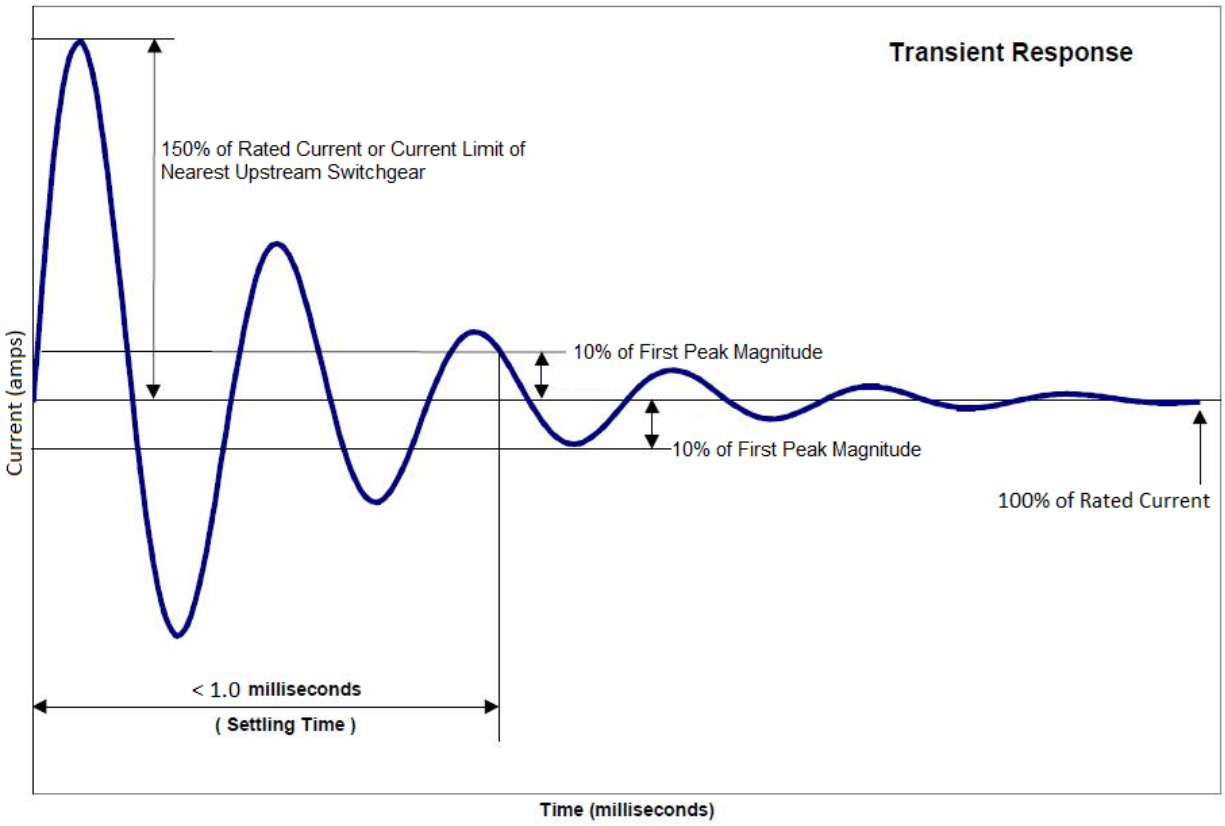


FIGURE 3.4.2-2: LARGE SIGNAL STABILITY TRANSIENT RESPONSE

3.4.2.1.4.2 EPCE INPUT IMPEDANCE

PWR28-2006

The EPCE input load impedance at the EPCE interface terminals shall be measured.

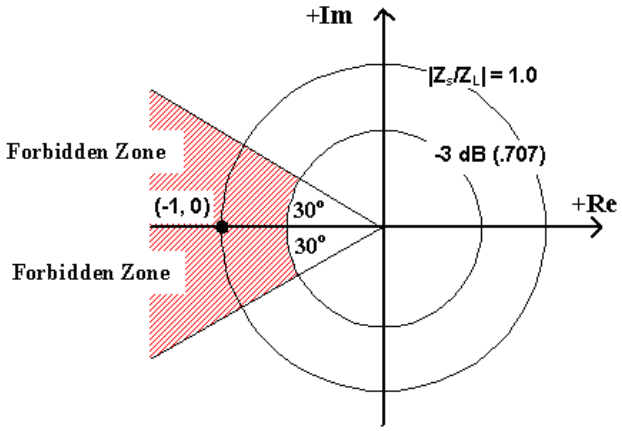
Rationale: The EPCE impedance value is required to calculate the stability margin of the source/load combination at the user input terminals. This document addresses a generic interface where the EPS and the EPCE have one common interface.

3.4.2.1.4.3 SMALL SIGNAL STABILITY

PWR28-2007

The EPCE shall maintain a complex impedance ratio of source impedance divided by load impedance (derived from [PWR120-1005], section 3.3.1.5.2) that remains outside the hatched area (Forbidden Zone) shown in Figure 3.4.2-3: Nyquist Stability Criteria, from 30 Hz to 100 kHz for all defined EPCE interfaces.

Rationale: The EPCE should meet this system-level requirement for small signal stability for all defined EPCE interfaces to maximize compatibility.



NOTE:

3. Z_S is the output impedance of the source subsystem.
4. Z_L is the input impedance of the load subsystem.

FIGURE 3.4.2-3: NYQUIST STABILITY CRITERIA

3.4.2.1.5 STARTUP AND INRUSH

3.4.2.1.5.1 CURRENT LIMITING SWITCHGEAR COMPATIBILITY

PWR28-2008

The EPCE shall be capable of operating from current limiting switchgear.

Rationale: Switchgear may limit the maximum input current to a value near the channel rating. EPCE with large values of energy storage (in capacitive filters or equivalent) will extend the rise time of the applied voltage as these filters charge. In extreme cases, the charging time may be greater than 100 ms. The EPCE must be compatible with this slow rise time. The EPCE should also try to minimize the amount of inrush/surge current seen by the switchgear.

3.4.2.1.5.2 INRUSH/SURGE CURRENT TRANSIENTS

PWR28-2009

The EPCE shall limit inrush/surge current to:

- 0.012 A*Sec / A for loads with currents 0A < I < 10A,
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a

margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 4286 microfarad (µF) for a 10 Amp source at 28 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 28 V = 4286µF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 28 V = 4286 µF.*

3.4.2.1.6 REVERSE CURRENT

PWR28-2010

The EPCE shall prevent reverse current flow back into the EPS source under normal operation for a fixed interface voltage.

Rationale: EPCE need to be designed to prevent current to out-flow into the power system under normal load operation with the voltage remaining constant. Loads, mainly motors and other inertial loads need to be designed as to not normally supply reverse currents (re-gen) into the distribution system and potentially raise the bus voltage to unacceptable levels causing the unintended tripping from other devices within the system. This requirement assumes a fixed steady state EPS bus voltage without any EPS droop in voltage therefore it is assumed that energy storage devices such as capacitors will not be affected by this requirement.

3.4.2.1.7 EPCE INPUT ISOLATION

PWR28-2011

The EPCE shall provide a minimum of 1 MΩ DC-resistive input isolation between each independent source input and between each source input and chassis.

Rationale: Maintain a consistent level of input isolation for EPCE and maintain isolation between power inputs such that no single failure within the EPCE will cause loss of electrical isolation between independent power buses or to chassis ground. These requirements apply to both supply and return circuits. Return isolation needs to be maintained when there are multiple circuits so as to not create a loop path (antenna), multiple return path (currents flowing through the single-point ground), or common mode currents. Isolation from chassis must be maintained to prevent currents through vehicle structure. Each EPCE must meet the failure requirements of the vehicle and should not cause loss of isolation between independent power busses.

3.4.2.2 ABNORMAL OPERATION

The EPCE is to return to normal operations after experiencing abnormal transients due to fault clearing identified in the following paragraphs. Abnormal transients occur when a malfunction or fault/failure is present in the system. The protective devices of the EPS,

during this condition, operate to isolate or remove the fault from the appropriate EPS interface and recover from the fault/failure.

3.4.2.2.1 ABNORMAL REVERSE CURRENTS

PWR28-2012

The EPCE shall limit reverse currents under abnormal conditions to:

- 0.012 A*Sec / A for loads with currents 0A < I < 10A;
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < I < 200A.

Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source/load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of a margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source.

*The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 4286 microfarad (µF) for a 10 Amp source at 28 VDC as determined by the equation: C = Q/V: C = 0.012sec*10A / 28 V = 4286µF.*

*There is no discontinuity at 10A as the 10A source in the second equation: ((0.00253sec*10A) + 0.0947) / 28 V = 4286 µF.*

3.4.2.2.2 OVERVOLTAGE SURGE

PWR28-2013

The EPCE shall meet the operational performance requirements as defined by the EPCE controlling documents after experiencing an overvoltage due to an EPS fault as shown in Figure 3.4.2-4: 28 VDC EPCE Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: This defines a worst-case overvoltage condition during fault clearing for major EPS faults. The user should not expect power quality during a fault condition. EPCE designers must take into account these conditions in the design of loads. EPCE designers need to select hardware to withstand anticipated worst-case overvoltage without permanently damaging system loads. EPCE controlling documents define how the equipment will operate nominally through the transient or recover to a safe state either automatically or by manual restart.

3.4.2.2.3 UNDERVOLTAGE SURGE

PWR28-2014

The EPCE shall meet the operational performance requirements as defined by the EPCE controlling documents after experiencing undervoltage due to an EPS fault as shown in Figure 3.4.2-4: 28 VDC EPCE Abnormal Voltage Limits for Overvoltage and Undervoltage.

Rationale: This event is defined at the EPCE interface. The user should not expect power quality during an EPS fault condition. The worst-case undervoltage condition will be outside of power quality while the system detects the fault, clears the condition, and re-establishes power to within power quality. Power quality will be re-established for users outside of the faulted area. EPCE controlling documents define how the equipment will operate nominally through the transient or recover to a safe state either automatically or by manual restart. The intent of this requirement is that loads should not be damaged or cause an unsafe condition as a result of undervoltage events. This requirement does not intend to stipulate whether any given load will be required to operate through the transient event or should configure to operate immediately following the event. The intent is to establish that the source may be removed such that all of the downstream EPCE may cease operating and will not be damaged. The EPCE input filter is not required to act as an uninterruptable power supply and any critical EPCE should have redundancy or multiple independent source inputs. Other considerations such as load criticality or system operational mode need to be used to determine recovery state. The EPCE can experience abnormal voltage droop and voltage overshoot greater than specified by the EPS, Normal Load Step Transient Voltage [PWR28-1009], section 3.3.3.1.2, while sharing an EPS source interface feeder with other loads. The magnitude of the abnormal voltage will be dependent on the loads applied and being applied/removed. Determination of the effects from the switching disturbances will be identified by the specific hardware controlling documents. It must be noted that this event is defined at the EPCE interface.

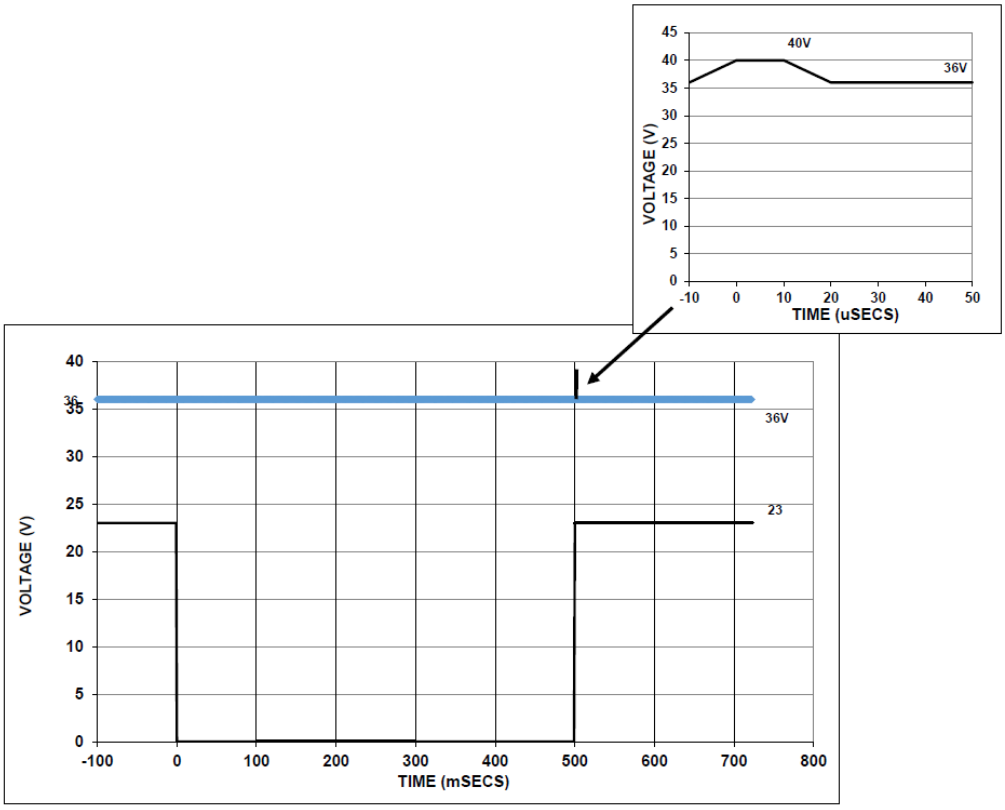


FIGURE 3.4.2-4: 28 VDC EPCE ABNORMAL VOLTAGE LIMITS FOR OVERVOLTAGE AND UNDERVOLTAGE

3.4.2.2.4 EMERGENCY OPERATION

PWR28-2015

EPCE deemed essential (contingency operations) shall continue to operate without loss of performance down to the reduced emergency voltage limit of 18V.

Rationale: Establish an emergency operation system voltage range. The voltage allows for contingency cases where the primary power generation source is disabled or unavailable to allow for 100% power system utilization. This requirement typically applies to unregulated sources (i.e., battery) where there are a few specified EPCE that are required to continue to operate below normal minimum voltages for contingency operations. Operations below this contingency voltage is usually not practical due to the source no longer able to supply the required current for the EPCE to operate. This requirement shall be tailored to account for system specific characteristics such as voltage drop and voltage droop.

4 VERIFICATION AND TESTING

It is the responsibility of the spacecraft developer to perform verification and validation. The majority of the standards will be verified using a combination of interface/compatibility testing, integrated end-to-end testing, and analysis at the subsystem and system-level. The following verification requirements represent best practices and may be tailored by the individual program as required to support their individual verification strategy.

The following provides guidance on verification methods.

An important part of achieving reliability and safety of the EPS is through verification performed at the appropriate level of assembly. This section is intended to identify critical electrical characteristics that need to be verified. This section provides the complete set of verification requirements necessary to ensure compliance with the interface and design requirements contained in the General Power Quality Requirements within sections 3.3 and 3.4.

The verification process and requirement closure are performed to ensure that the product complies with the requirement as specified and as determined by the verification requirement. Sections 4.1 and 4.2 contain a verification requirement for each requirement in sections 3.3 and 3.4 respectively.

The intent is to establish verification of spacecraft power sources (EPS) with clean, resistive loads, and to establish verification for spacecraft loads (EPCE) with clean, battery-like sources.

A - Analysis is a method of verification utilizing techniques and tools such as computer and hardware simulations, analog modeling, similarity assessments, and validation of records to confirm that design requirements to be verified have been satisfied. Analysis is the evaluation of the results of multiple tests and analyses at a lower level as it would apply to a higher level of assembly. When analysis is selected as the verification method, the chosen analytical methodology will be supported by appropriate rationale and be detailed in the applicable documents.

D - Demonstration is a qualitative exhibition of functional performance (i.e., serviceability, accessibility, transportability, and human engineering features) usually accomplished with no or minimal instrumentation.

I - Inspection is a method of verification of physical characteristics that determines compliance of the item with requirements without the use of special laboratory equipment, procedures, test support items, or services. Inspection uses standard methods such as visuals, gauges, etc. to verify compliance with requirements. Hardware may be inspected for the following:

- Construction;
- Workmanship;
- Physical condition;

- Specification and/or drawing compliance.

Inspection may be used to confirm that engineering drawings call out proper design and construction features (e.g., materials and processes). Inspection includes Review of Design (ROD). This is typically a review of the as-built drawings to confirm that a design feature has been incorporated into the design.

T - Test is a method of verification wherein requirements are verified by measurement during or after the controlled application of functional and environmental stimuli. These measurements may require the use of laboratory equipment, recorded data, procedures, test support items, or services. All verification, qualification, and acceptance test activities, pass or fail test criteria or acceptance tolerance bands (based upon design and performance requirements) shall be specified prior to conducting the test. This will ensure that the actual performance of tested equipment or systems meets or exceeds specifications.

4.1 ELECTRICAL POWER SYSTEM, SOURCE POWER INTERFACE

4.1.1 EPS SYSTEM CHARACTERISTICS

4.1.1.1 SINGLE-POINT GROUND

PWR120-1001V, PWR28-1001V

Verification of single point ground shall be performed by analysis and inspection. An analysis and inspection of all production electrical wiring drawings shall be performed to verify that the power distribution system maintains a single point ground.

4.1.1.2 DISTRIBUTION WIRING

PWR120-1002V, PWR28-1002V

Verification of two-wire distribution shall be performed by analysis and inspection. An analysis and inspection of all production electrical wiring drawings shall be performed to verify that the power distribution system maintains a two-wire system. The verification shall be considered successful when the analysis and inspection shows that the EPS utilizes a two-wire system as specified in the requirement [PWR120-1002] and [PWR28-1002].

4.1.1.3 ISOLATION

PWR120-1003V, PWR28-1003V

Verification of power bus isolation between two or more independent EPS power buses shall be performed by analysis, inspection, and test. An analysis and inspection of production drawings and hardware configuration end item input isolation data shall be performed to verify that the supply line of each channel and return line (excluding single-point ground connection points) of each channel are not connected. Tests shall be performed on subassemblies and cabling to verify source isolation. The verification shall be considered successful when the analysis, inspection, and tests show that the isolation between supply lines of each channel and return lines (excluding single-point

ground connection points) of each channel are isolated as specified in the requirements [PWR120-1003] and [PWR28-1003].

Rationale: Inspection alone may not fully verify circuit performance and workmanship or identify damage to the source isolation design. Tests to perform isolation verification of energized integrated multiple sources within a vehicle may not be practical or feasible but should be performed on a subassembly level and on cabling to verify the isolation requirements [PWR120-1003] and [PWR28-1003].

4.1.1.4 REVERSE CURRENT

PWR120-1004V, PWR28-1004V

No Verification Required (NVR)

Rationale: No EPS verification required under normal operations since there is no EPCE reverse current allowed. However, under abnormal operations the EPS will need to meet the EPCE abnormal reverse current as defined under requirements [PWR120-1015] and [PWR28-1015].

4.1.1.5 STABILITY

4.1.1.5.1 SOURCE IMPEDANCE

PWR120-1005V, PWR28-1005V

The EPS source impedance shall be determined by test and analysis. See Appendix Section F0.

4.1.1.5.2 SMALL SIGNAL STABILITY – SYSTEM STABILITY

PWR120-1006V, PWR28-1006V

Verification of small signal stability shall be performed by analysis and test of source and load impedances. An analysis shall be performed based on the Nyquist Criteria shown in requirements [PWR120-1006] and [PWR28-1006].

4.1.1.6 ELECTROMAGNETIC COMPATIBILITY

PWR120-1007V, PWR28-1007V

Verification shall be performed by completing the analyses and tests per EMI Control Plan in accordance with the vehicle mission requirements.

Rationale: Adopt a common EMI requirement for the power system.

4.1.2 120V EPS CHARACTERISTICS

4.1.2.1 NORMAL OPERATION REQUIREMENTS

4.1.2.1.1 STEADY-STATE VOLTAGE

PWR120-1008V

Verification of compatibility with the steady-state voltage range shall be performed by test.

The steady-state voltage shall be measured under a no-load open circuit condition and when subjected to a resistive load at 100% of rated capacity. The verification shall be considered successful when the test shows that the EPS provided steady-state voltage is within the range specified in requirement [PWR120-1008] for the EPCE power interface.

Any EPS power interface defined upstream of the EPCE power interface shall also include the necessary voltage drop margins to maintain the range specified in requirement [PWR120-1008] for the downstream EPCE power interface.

Rationale: Minimum load condition is the initial powered up state of the system.

4.1.2.1.2 NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR120-1009V

Verification of compatibility with the normal load step transient shall be performed by test.

A test shall be performed to verify that the voltage remains within the magnitude and duration limits specified in requirement [PWR120-1009] when subjected to a 50% (±5%) representative load change including application and removal of the load with a nominal initial voltage within the range specified. The representative load shall be 50% (±5%) of the rated output power. The test shall be performed in two parts. The first part shall consist of the application and removal of the load with the EPS operating at 10% (±5%) of nominal operating mode power capacity. The second part shall consist of the application and removal of the load with the power system operating at 45% (±5%) of nominal operating mode power capacity. The verification shall be considered successful when the tests show that the voltage remains within the range specified in requirement [PWR120-1009].

Any EPS power interface defined upstream of the EPCE power interface shall also include the necessary voltage drop margins to maintain the range specified in requirement [PWR120-1009] for the downstream EPCE power interface.

Rationale: This normal load step test should be conducted under nominal system operating conditions and should not be considered a turn-on or turn-off transient test. The test conditions are at the load interface.

4.1.2.1.3 RIPPLE VOLTAGE

4.1.2.1.3.1 PEAK RIPPLE VOLTAGE

PWR120-1010V

Verification of the peak ripple voltage shall be performed by test. A test shall be performed to verify that the maximum peak ripple voltage is less than limits specified in requirement [PWR120-1010] when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the maximum peak ripple voltage is in accordance with requirement [PWR120-1010].

Rationale: Maximum peak ripple voltage is useful as a primary power quality parameter so components can be properly sized to withstand peak voltages within the system. Loads that are to be connected to the power system are considered representative loads. This requirement is intended to be verified under lab conditions using a representative interface source and load. Design-specific power specifications may allocate the ripple for the EPS itself at specified upper-tier EPS interfaces, including the generic EPS/EPCE interface.

4.1.2.1.3.2 RIPPLE VOLTAGE AMPLITUDE

PWR120-1011V

Verification of the ripple voltage amplitude shall be performed by test. A test shall be performed to verify that the maximum rms ripple voltage is less than limits specified in requirement [PWR120-1011] when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the maximum ripple voltage is in accordance with requirement [PWR120-1011].This measurement shall be made using a true rms voltmeter with a bandwidth of at least 1 MHz.

Rationale: Maximum rms ripple voltage is useful as a primary power quality parameter to determine how much "AC noise" is present in the DC system. Loads that are to be connected to the power system are considered representative loads. Ripple voltage includes the collective contributions from sources and loads at EPS Interface as a primary power quality parameter. Design-specific power specifications may allocate the ripple for the EPS itself at specified upper-tier EPS interfaces, including the generic EPS/EPCE interface.

4.1.2.1.3.3 RIPPLE VOLTAGE SPECTRUM

PWR120-1012V

Verification of the ripple voltage spectrum shall be performed by test. A test shall be performed to verify that the ripple voltage remains within the magnitude and frequency limits specified in requirement [PWR120-1012] when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be

considered successful when the test shows that the ripple voltage is within the range specified in requirement [PWR120-1012].

Rationale: Ripple voltage is useful as a primary power quality parameter to determine how much "AC noise" is present in the DC system over a defined frequency spectrum. Ripple voltage includes the collective contributions from sources and loads at the EPS Source interface as a primary power quality parameter. The frequency domain limit of the cumulative noise is maintained at least 6dB below the Electromagnetic Compatibility (EMC) conducted susceptibility requirements of MIL-STD-461. Design-specific power specifications may allocate the ripple for the EPS itself at specific defined interfaces, not just at the generic EPS/EPCE interface.

4.1.2.1.4 EXTERNAL POWER SOURCE

PWR120-1013V

External power sources shall be tested to verify compliance with this standard.

4.1.2.1.5 INRUSH/SURGE CURRENT TRANSIENTS

PWR120-1014V

Verification of EPS inrush capability shall be performed by test. The test shall be performed by charging the specified equivalent capacitance without causing a trip of the controlling switchgear.

4.1.2.2 ABNORMAL OPERATION

4.1.2.2.1 ABNORMAL REVERSE CURRENT

PWR120-1015V

Verification that the EPS can accept the abnormal EPCE reverse current without damage shall be performed by test. The verification shall be considered successful when analysis of test results show that no EPS is damaged by the abnormal reverse current flow as specified in the requirement [PWR120-1015].

4.1.2.2.2 EPS FAULT PROTECTION

PWR120-1016V

Verification of overcurrent protection shall be verified by test. The test shall consist of loading the EPS source interface with resistive loads until the overcurrent protection clears the overcurrent condition. The verification shall be considered successful when analysis of the test results show the EPS source interface clears the overcurrent condition.

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight-like configurations

using appropriate circuit cables/connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

4.1.2.2.3 OVERVOLTAGE SURGE

PWR120-1017V

Verification of the overvoltage surge due to EPS fault shall be verified by test or analysis. The test or analysis shall be performed to verify the overvoltage surge at the EPS source side of the load interface remains within the limits specified in the requirement [PWR120-1017] when subjected to the application and removal of a high current fault or other component failure. An analysis shall be performed to evaluate fault conditions where testing is not possible and could degrade flight hardware. The verification shall be considered successful when the test or analysis shows the overvoltage at the EPS source interface is within the range specified in requirement [PWR120-1017].

Rationale: This verification of the source surge is at the EPCE interface. Application and removal of a fault within the EPS can result in an overvoltage condition on other interface channels due to the line inductance between the source and the load.

4.1.2.2.4 UNDERVOLTAGE SURGE

PWR120-1018V

Verification of the undervoltage surge due to EPS fault shall be verified by test or analysis. The test or analysis shall be performed to verify the undervoltage surge at the EPS source side of the load interface remains within the limits specified in the requirement [PWR120-1018] when subjected to the application and removal of a high current fault or other component failure. An analysis shall be performed to evaluate fault conditions where testing is not possible and could degrade flight hardware. The verification shall be considered successful when the test or analysis shows the undervoltage at the EPS source interface is within the range specified in requirement [PWR120-1018].

Rationale: This verification of the source undervoltage is at the EPCE interface. Application and removal of a fault within the EPS can result in an undervoltage condition on other interface channels due to the line inductance between the source and the load.

4.1.2.2.5 EMERGENCY OPERATION

PWR120-1019V

Verification of EPS Emergency Operation shall be performed by analysis. The analysis shall verify that the EPS control and protection logic allows access to all available power sources during fault or component failure conditions.

4.1.2.2.6 FAULTS

4.1.2.2.6.1 HIGH IMPEDANCE FAULTS

PWR120-1020V

Verification of high impedance fault protection shall be performed by test. The test shall consist of loading the EPS with a resistive load. The verification shall be considered successful when the test shows that the EPS clears the overcurrent condition within the time specified in the requirement [PWR120-1020].

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight-like configurations using appropriate circuit cables/connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

4.1.2.2.6.2 HIGH CURRENT FAULTS

PWR120-1021V

Verification of high current fault protection shall be performed by test. The test shall consist of loading the EPS with a resistive load. The verification shall be considered successful when the test shows that the EPS clears the overcurrent condition within the time specified in the requirement [PWR120-1021] .

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight-like configurations using appropriate circuit cables/connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

4.1.2.2.6.3 EPS FAULT CONTAINMENT

PWR120-1022V

Verification of EPS fault containment shall be performed by analysis. The analysis shall consist of evaluating all branch circuits to verify that overcurrent protection is provided, and trip coordination will prevent fault propagation and isolate faults. The verification shall be considered successful when the analysis shows that fault containment meets the requirement [PWR120-1022].

4.1.3 28V EPS CHARACTERISTICS

4.1.3.1 NORMAL OPERATION REQUIREMENTS

4.1.3.1.1 STEADY-STATE VOLTAGE

PWR28-1008V

Verification of compatibility with the steady-state voltage range shall be performed by test.

The steady-state voltage shall be measured under a no-load open circuit condition and when subjected to a resistive load at 100% of rated capacity. The verification shall be considered successful when the test shows that the EPS provided steady-state voltage is within the range specified in requirement [PWR28-1008] for the EPCE power interface.

Any EPS power interface defined upstream of the EPCE power interface shall also include the necessary voltage drop margins to maintain the range specified in requirement [PWR28-1008] for the downstream EPCE power interface.

Rationale: Minimum load condition is the initial powered up state of the system.

4.1.3.1.2 NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR28-1009V

Verification of compatibility with the normal load step transient shall be performed by test.

A test shall be performed to verify that the voltage remains within the magnitude and duration limits specified in the requirement [PWR28-1009] when subjected to a 50% (±5%) representative load change including application and removal of the load with a nominal initial voltage within the range specified. The representative load shall be 50% (±5%) of the rated output power. The test shall be performed in two parts. The first part shall consist of the application and removal of the load with the EPS operating at 10% (±5%) of nominal operating mode power capacity. The second part shall consist of the application and removal of the load with the power system operating at 45% (±5%) of nominal operating mode power capacity. The verification shall be considered successful when the tests show that the voltage remains within the range specified in requirement [PWR28-1009].

Any EPS power interface defined upstream of the EPCE power interface shall also include the necessary voltage drop margins to maintain the range specified in requirement [PWR28-1009] for the downstream EPCE power interface.

Rationale: This normal load step test should be conducted under nominal system operating conditions and should not be considered a turn-on or turn-off transient test. The test conditions are at the load interface.

4.1.3.1.3 RIPPLE VOLTAGE

4.1.3.1.3.1 PEAK RIPPLE VOLTAGE

PWR28-1010V

Verification of the peak ripple voltage shall be performed by test. A test shall be performed to verify that the maximum peak ripple voltage is less than limits specified in requirement [PWR28-1010]. when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when

the test shows that the maximum peak ripple voltage is in accordance with requirement [PWR28-1010].

Rationale: Maximum peak ripple voltage is useful as a primary power quality parameter so components can be properly sized to withstand peak voltages within the system. Loads that are to be connected to the power system are considered representative loads. This requirement is intended to be verified under lab conditions using a representative interface source and load. Design-specific power specifications may allocate the ripple for the EPS itself at specified upper-tier EPS interfaces, including the generic EPS/EPCE interface.

4.1.3.1.3.2 RIPPLE VOLTAGE AMPLITUDE

PWR28-1011V

Verification of the ripple voltage amplitude shall be performed by test. A test shall be performed to verify that the maximum rms ripple voltage is less than limits specified in the requirement [PWR28-1011] when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the maximum ripple voltage is in accordance with requirement [PWR28-1011]. This measurement shall be made using a true rms voltmeter with a bandwidth of at least 1 MHz.

Rationale: Maximum rms ripple voltage is useful as a primary power quality parameter to determine how much "AC noise" is present in the DC system. Loads that are to be connected to the power system are considered representative loads. Ripple voltage includes the collective contributions from sources and loads at EPS Interface as a primary power quality parameter. Design-specific power specifications may allocate the ripple for the EPS itself at specified upper-tier EPS interfaces, including the generic EPS/EPCE interface.

4.1.3.1.3.3 RIPPLE VOLTAGE SPECTRUM

PWR28-1012V

Verification of the ripple voltage spectrum shall be performed by test. A test shall be performed to verify that the ripple voltage remains within the magnitude and frequency limits specified in the requirement [PWR28-1012] when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the ripple voltage is within the range specified in requirement [PWR28-1012].

Rationale: Ripple voltage is useful as a primary power quality parameter to determine how much "AC noise" is present in the DC system over a defined frequency spectrum. Ripple voltage includes the collective contributions from sources and loads at the EPS Source interface as a primary power quality parameter. The frequency domain limit of the cumulative noise is maintained at least 6dB below the Electromagnetic Compatibility (EMC) conducted susceptibility requirements of MIL-STD-461. Design-specific power

specifications may allocate the ripple for the EPS itself at specific defined interfaces, not just at the generic EPS/EPCE interface.

4.1.3.1.4 EXTERNAL POWER SOURCE

PWR28-1013V

External power sources shall be tested to verify compliance with this standard.

4.1.3.1.5 INRUSH/SURGE CURRENT TRANSIENTS

PWR28-1014V

Verification of EPS inrush capability shall be performed by test. The test shall be performed by charging the specified equivalent capacitance without causing a trip of the controlling switchgear.

4.1.3.2 ABNORMAL OPERATION

4.1.3.2.1 ABNORMAL REVERSE CURRENT

PWR28-1015V

Verification that the EPS can accept the abnormal EPCE reverse current without damage shall be performed by test. The verification shall be considered successful when analysis of test results show that no EPS is damaged by the abnormal reverse current flow as specified in the requirement [PWR28-1015].

4.1.3.2.2 EPS FAULT PROTECTION

PWR28-1016V

Verification of overcurrent protection shall be verified by test. The test shall consist of loading the EPS source interface with resistive loads until the overcurrent protection clears the overcurrent condition. The verification shall be considered successful when analysis of the test results show the EPS source interface clears the overcurrent condition.

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight-like configurations using appropriate circuit cables/connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

4.1.3.2.3 OVERVOLTAGE SURGE

PWR28-1017V

Verification of the overvoltage surge due to EPS fault shall be verified by test or analysis. The test or analysis shall be performed to verify the overvoltage surge at the EPS source side of the load interface remains within the limits specified in the

requirement [PWR28-1017] when subjected to the application and removal of a high current fault or other component failure. An analysis shall be performed to evaluate fault conditions where testing is not possible and could degrade flight hardware. The verification shall be considered successful when the test or analysis shows the overvoltage at the EPS source interface is within the range specified in requirement [PWR28-1017].

Rationale: This verification of the source surge is at the EPCE interface. Application and removal of a fault within the EPS can result in an overvoltage condition on other interface channels due to the line inductance between the source and the load.

4.1.3.2.4 UNDERVOLTAGE SURGE

PWR28-1018V

Verification of the undervoltage surge due to EPS fault shall be verified by test or analysis. The test or analysis shall be performed to verify the undervoltage surge at the EPS source side of the load interface remains within the limits specified in the requirement [PWR28-1018] when subjected to the application and removal of a high current fault or other component failure. An analysis shall be performed to evaluate fault conditions where testing is not possible and could degrade flight hardware. The verification shall be considered successful when the test or analysis shows the undervoltage at the EPS source interface is within the range specified in requirement [PWR28-1018].

Rationale: This verification of the source undervoltage is at the EPCE interface. Application and removal of a fault within the EPS can result in an undervoltage condition on other interface channels due to the line inductance between the source and the load.

4.1.3.2.5 EMERGENCY OPERATION

PWR28-1019V

Verification of EPS Emergency Operation shall be performed by analysis. The analysis shall verify that the EPS control and protection logic allows access to all available power sources during fault or component failure conditions.

4.1.3.2.6 FAULTS

4.1.3.2.6.1 HIGH IMPEDANCE FAULTS

PWR28-1020V

Verification of high impedance fault protection shall be performed by test. The test shall consist of loading the EPS with a resistive load. The verification shall be considered successful when the test shows that the EPS clears the overcurrent condition within the time specified in the requirement [PWR28-1020].

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight-like configurations using appropriate circuit cables/connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

4.1.3.2.6.2 HIGH CURRENT FAULTS

PWR28-1021V

Verification of high current fault protection shall be performed by test. The test shall consist of loading the EPS with a resistive load. The verification shall be considered successful when the test shows that the EPS clears the overcurrent condition within the time specified in the requirement [PWR28-1021].

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight-like configurations using appropriate circuit cables/connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

4.1.3.2.6.3 EPS FAULT CONTAINMENT

PWR28-1022V

Verification of EPS fault containment shall be performed by analysis. The analysis shall consist of evaluating all branch circuits to verify that overcurrent protection is provided, and trip coordination will prevent fault propagation and isolate faults. The verification shall be considered successful when the analysis shows that fault containment meets the requirement [PWR28-1022].

4.2 ELECTRIC POWER CONSUMING EQUIPMENT INTERFACE

4.2.1 120V EPCE CHARACTERISTICS

4.2.1.1 NORMAL OPERATION

4.2.1.1.1 STEADY STATE OPERATION

PWR120-2002V

Verification of EPCE operational compatibility with the steady-state voltage range shall be performed by test. Verification shall be performed by test at low and high input voltage values as specified in requirement [PWR120-2001]. EPCE shall be operated under selected loading conditions that envelop operational loading.

For 120 VDC systems, the acceptable method to demonstrate compatibility with the minimum and maximum system voltage level is to test the EPCE at a steady-state input voltage of 98 VDC (or below) and 136 VDC (or above).

The verification shall be considered successful when the test shows the EPCE operates nominally.

Rationale: EPCE undergoing susceptibility testing typically test at the low and high voltage with a voltage ripple superimposed.

4.2.1.1.2 EPCE POWER INTERFACE, NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR120-2002V

Verification of compatibility with the normal load step transient at the EPS/EPCE interface shall be performed by test. Verification shall be performed by test at low and high input voltage values as specified in requirement [PWR120-2002]. EPCE shall be operated under selected loading conditions that envelop operational loading. Rate of change should be between 0.5 Volts per microsecond (V/μsec) and 1 V/μsec to prevent degradation of flight hardware (i.e. fuse fatigue).

For 120 VDC systems, EPCE should be tested by applying an input voltage transient step as shown in Figure 4.2.1-1: 120 VDC Normal Load Step-Down Transient Test and Figure 4.2.1-2: 120 VDC Normal Load Step-Up Transient Test from the nominal steady-state voltage (120 VDC) to the maximum transient levels (141 VDC) and from a steady-state voltage of 120 VDC to the minimum transient levels (93 VDC). The verification shall be considered successful when the test shows the EPCE operates nominally when input terminals are subjected to test voltages as specified below in Figure 4.2.1-1: 120 VDC Normal Load Step-Down Transient Test and Figure 4.2.1-2: 120 VDC Normal Load Step-Up Transient Test.

Rationale: The test conditions are at the load interface.

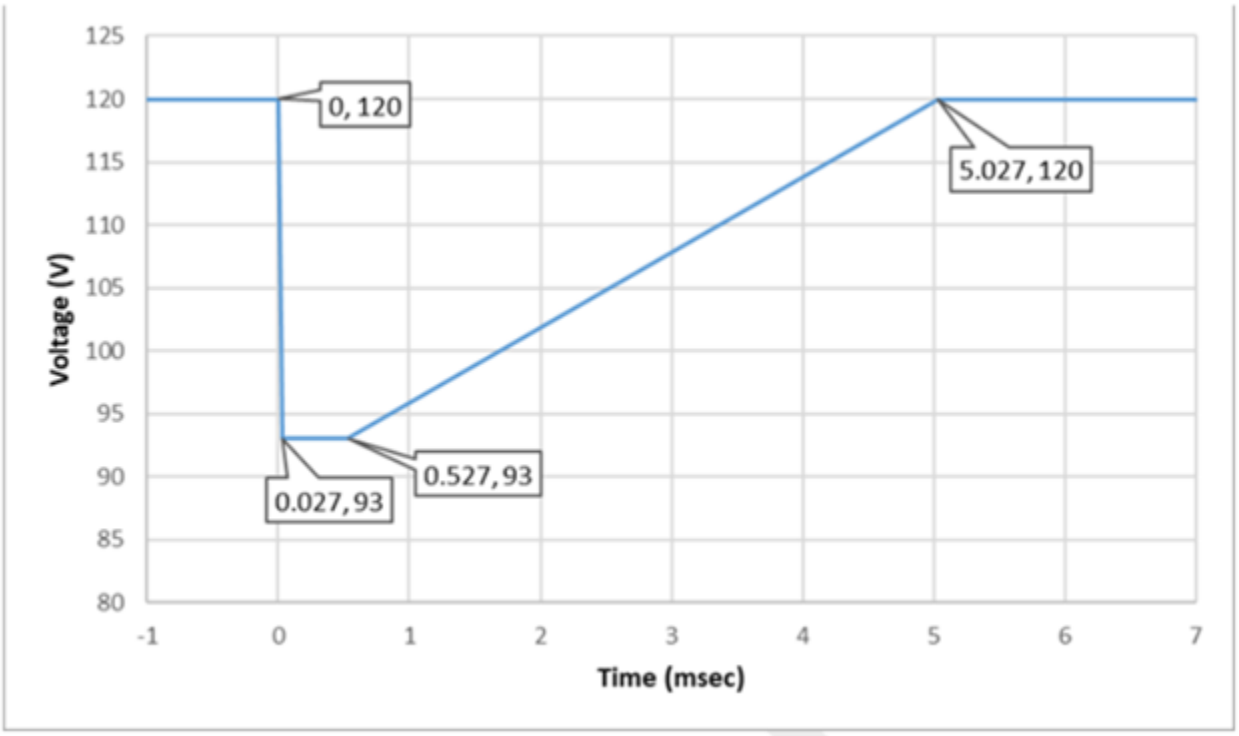


FIGURE 4.2.1-1: 120 VDC NORMAL LOAD STEP-DOWN TRANSIENT TEST

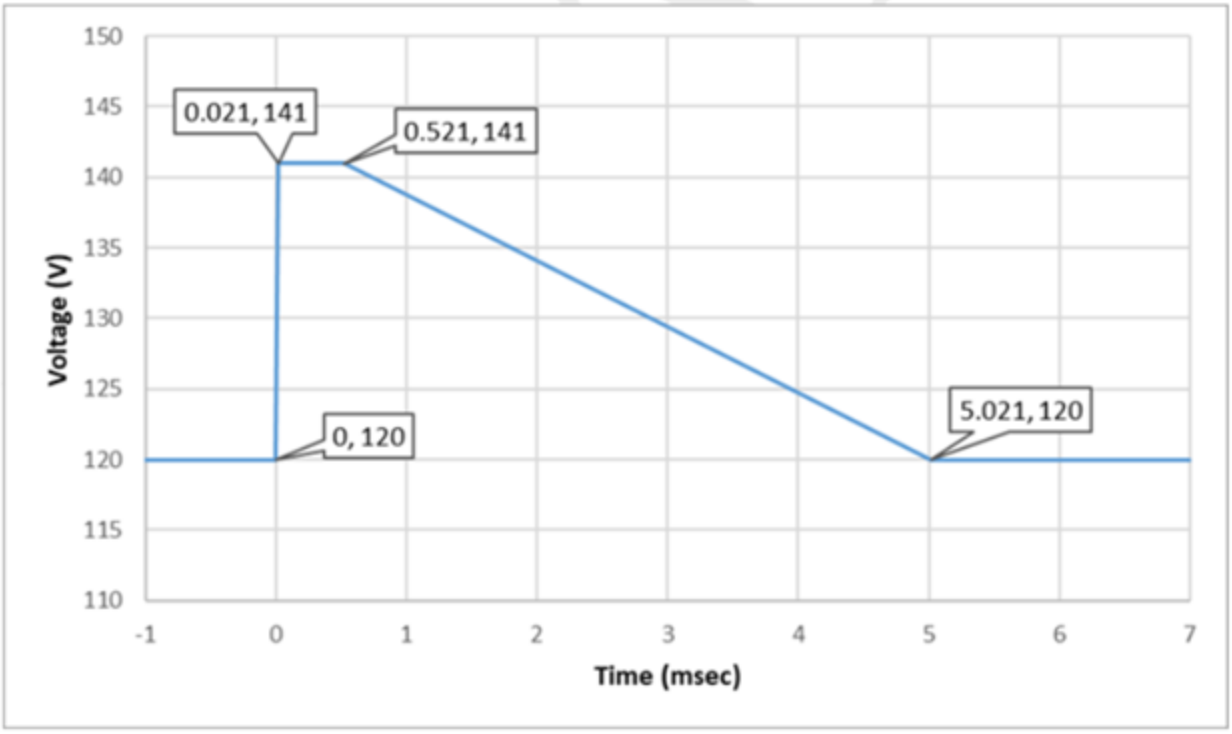


FIGURE 4.2.1-2: 120 VDC NORMAL LOAD STEP-UP TRANSIENT TEST

4.2.1.1.3 EPCE RIPPLE COMPATABILITY

4.2.1.1.3.1 EPCE, RIPPLE CURRENT

PWR120-2003V

NVR

Rationale: Verification is considered successful by successfully performing the ripple tests as defined by the EMI control document.

4.2.1.1.3.2 EPCE, RIPPLE VOLTAGE SPECTRUM

PWR120-2004V

NVR

Rationale: Verification is considered successful by successfully performing the spectrum tests as defined by the EMI control document.

4.2.1.1.4 STABILITY

4.2.1.1.4.1 LARGE SIGNAL STABILITY

PWR120-2005V

Large signal stability shall be verified by test and analysis.

A large signal stability test shall be conducted for EPCE connected to the EPS source interface. An integrated analysis shall be provided for representative maximum and minimum load cases to demonstrate that impedance variations will not impact system stability. The input and transient response waveforms for the EPCE shall be recorded from the start of the pulse through the time when the transient diminishes to, and remains below, 10 percent of the maximum amplitude of the response. The input waveform shall be measured at the secondary side of the injection transformer.

The required test conditions may be produced using a programmable power source or the setup shown in Appendix Section E.5. Short-duration voltage pulses, as defined below, shall be applied. Short-duration power-system transients are defined, as part of the Large Signal Stability requirement, as follows:

1. The rise and fall times (between 10 and 90 percent of the amplitude points) of the input voltage pulse shall be less than 1 microsecond.

2. Duration of the voltage pulse may vary between 20 microseconds and 125 microseconds in duration. In test, this shall be satisfied by applying pulses of duration of 20, 50, 80, 100, and 125 microseconds (±5 microseconds).

3. Magnitude of the voltage pulses imposed on top of the 120.0 ± 1.0 VDC input shall be selected such that

    a. The peak current transient is 50% above full-load current or is at the current limit of the nearest upstream switchgear.

    b. The resulting imposed voltage magnitude remains within the EPS normal load step transient limits.

The defined transient is illustrated in Figure 4.2.1-3: Large Signal Stability Test Transient and appears in series with the output of the power source as shown in Appendix Section E.5.

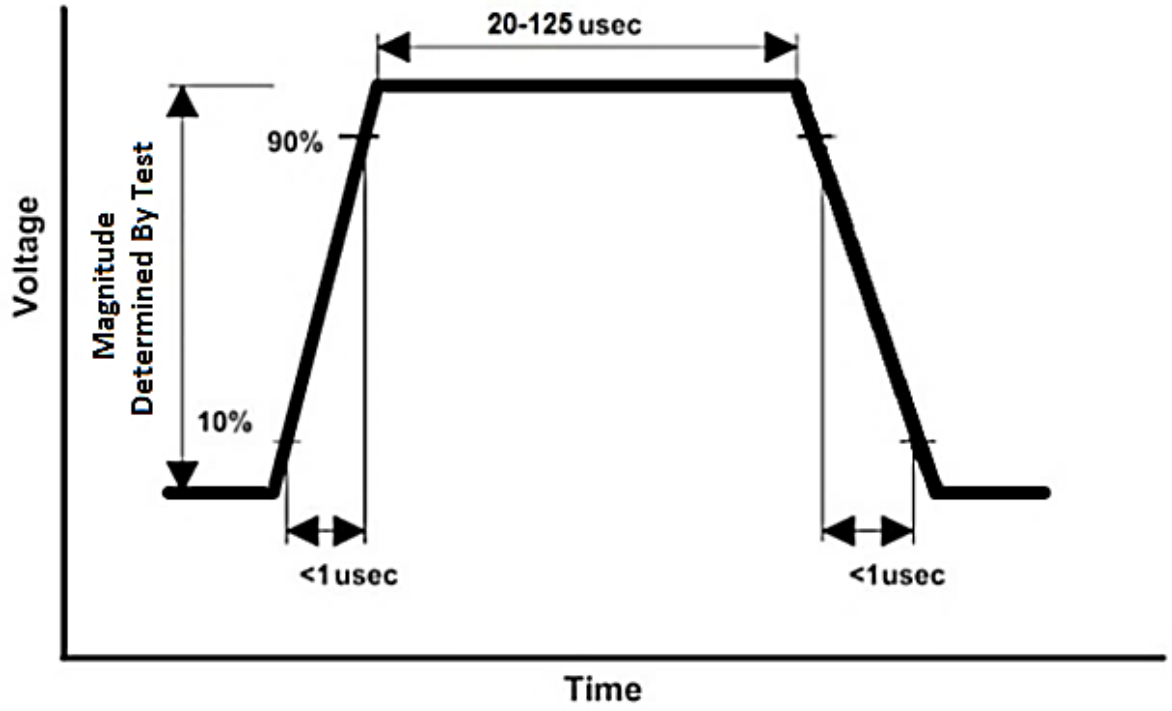


FIGURE 4.2.1-3: LARGE SIGNAL STABILITY TEST TRANSIENT

The verification shall be considered successful when results show that transient responses, measured at the input to EPCE, diminish to 10 percent of the maximum amplitude within 1.0 milliseconds and remain below 10 percent thereafter as illustrated in Figure 3.4.1-2: Large Signal Stability Transient Response. The connected EPCE shall maintain full performance as specified during the resulting transients.

For the analysis method of verification, the analysis model must be a high-fidelity time domain model (which includes the voltage and/or current control loops of the converter) in order to properly capture the voltage transient response when subjected to the large signal stability pulse.

4.2.1.1.4.2 EPCE INPUT IMPEDANCE

PWR120-2006V

Verification of EPCE input impedance shall be performed by test. See Appendix Section 0. EPCE impedance shall be verified by measuring the normalized input impedance magnitude and phase at low and high input voltage values as specified in the requirement [PWR120-2006].

Rationale: This requirement needs to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same EPCE.

4.2.1.1.4.3 SMALL SIGNAL STABILITY

PWR120-2007V

Verification of EPCE small signal stability at the EPS source interface shall be performed by test and analysis. EPCE small signal stability shall be verified by calculating the complex impedance ratio of the source impedance divided by the load impedance and ensuring that it remains outside the hatched area (Forbidden Zone) shown in Figure 3.3.1-1: Nyquist Stability Criteria, from 30 Hz to 100 kHz. EPCE shall be operated under selected loading conditions that envelop operational loading. The verification shall be considered successful when the analysis supported by test data shows the Z_S divided by Z_L ratio for all defined EPCE interfaces do not cross into the Forbidden Zone defined in requirement [PWR28-2007].

Rationale: This requirement needs to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same EPCE. A basic calculation example and test setup for input impedance tests to measure both magnitude and phase curves are described in Appendix Section F.4.

4.2.1.1.5 STARTUP AND INRUSH

4.2.1.1.5.1 CURRENT LIMITING SWITCHGEAR COMPATIBILITY

PWR120-2008V

Verification of the current limiting source compatibility shall be by test. The test shall consist of operating the device under test (DUT) being fed by current limiting switchgear that limits the current to 110% of the switchgear rating. The DUT shall not exhibit any malfunction, degradation of performance, or deviation from specified parameters when operated per requirement [PWR120-2008].

4.2.1.1.5.2 INRUSH/SURGE CURRENT TRANSIENTS

PWR120-2009V

Verification of allowable EPCE inrush and surge transient shall be performed by test and analysis using a characteristic non-current limiting source and a source that limits current to 110% of the test current as the test source. The test or analysis shall be performed as illustrated in Appendix Section E.2 to verify that the DUT inrush current during initial voltage application and surge current during DUT operation remains within the magnitude and duration limits specified in requirement [PWR120-2009] when using the non-current limiting and current limiting (110%) source. The verification shall be considered successful when the tests and analysis show that the transient remains within the limits specified in the requirement [PWR120-2009].

4.2.1.1.6 REVERSE CURRENT

PWR120-2010V

Verification of EPCE reverse current shall be performed by test and analysis. The test and analysis shall be performed on EPCE circuitry to show that, during normal operation, there are no reverse currents that will flow from the EPCE back into the EPS. The test and analysis shall be performed as illustrated in Appendix Section E.2. The analysis shall be considered successful when the tests and analysis show that no EPCE reverse current flows as specified in the requirement [PWR120-2010].

4.2.1.1.7 EPCE INPUT ISOLATION

PWR120-2011V

Verification of power source isolation shall be performed by test and analysis. EPCE equipment shall be tested to the specified limits for dielectric isolation between power sources and between power sources and chassis. Analysis of the design shall be performed to determine no single failure can cause loss of isolation.

4.2.1.2 ABNORMAL OPERATION

4.2.1.2.1 ABNORMAL REVERSE CURRENTS

PWR120-2012V

Verification of EPCE reverse current shall be performed by test and analysis. The test and analysis shall be performed as illustrated in Appendix Section E.2 on EPCE circuitry to determine the amount of current that will flow from the EPCE back into EPS during a simulated system voltage droop and EPS fault condition. The test or analysis shall be considered successful when the test and analysis show that EPCE limits reverse current flow as specified in the requirement [PWR120-2012].

4.2.1.2.2 OVERVOLTAGE SURGE

PWR120-2013V

Verification of compatibility with the overvoltage surge at the EPS load interface shall be performed by test and analysis.

For 120 VDC systems, EPCE should be tested from the nominal steady-state voltage (120 VDC) to the maximum transient levels (150 VDC), and back to the nominal steady-state voltage (120 VDC), as specified in requirement [PWR120-2013]. Figure 4.2.1-4: 120 VDC Overvoltage Transient Test Waveform depicts the voltage and time steps. The test and analysis shall be performed with the EPCE subjected to an input transient with a maximum rate of change should be between 9.5 V/µsec and 10.5 V/µsec. The verification shall be considered successful when the test and analysis shows the EPCE operates nominally per the EPCE controlling documents after subjected to the overvoltage surge as specified in requirement [PWR120-2013].

Rationale: This verification of the source surge is at the EPCE interface.

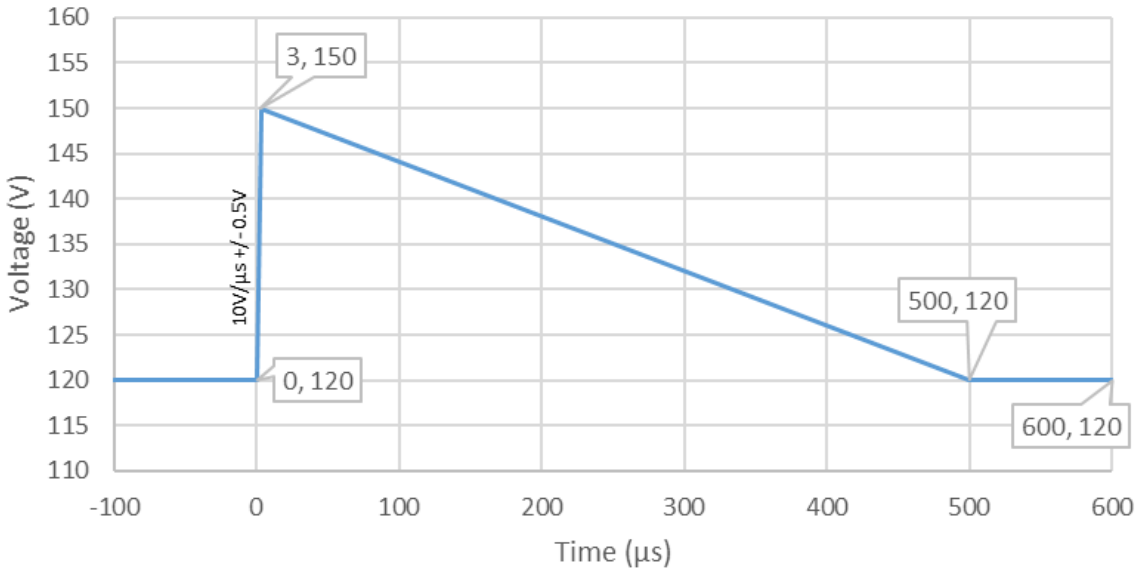


FIGURE 4.2.1-4: 120 VDC OVERVOLTAGE TRANSIENT TEST WAVEFORM

4.2.1.2.3 UNDERVOLTAGE SURGE

PWR120-2014V

The test shall be performed with the EPCE subjected to an input transient as specified in requirement [PWR120-2014]. EPCE should be tested from the steady-state voltage (120 VDC) to 0 VDC and back to the steady-state voltage (120 VDC). Figure 4.2.1-5: 120 VDC Undervoltage Transient Test Waveform depicts the voltage and time steps. The rate of change should be between 9.5 V/µsec and 10.5 V/µsec. The verification shall be considered successful when the analysis of the test results shows the EPCE operates nominally per the EPCE controlling documents after being subjected to the undervoltage surge as specified in requirement [PWR120-2014].

Rationale: This verification of the source undervoltage is at the EPCE interface.

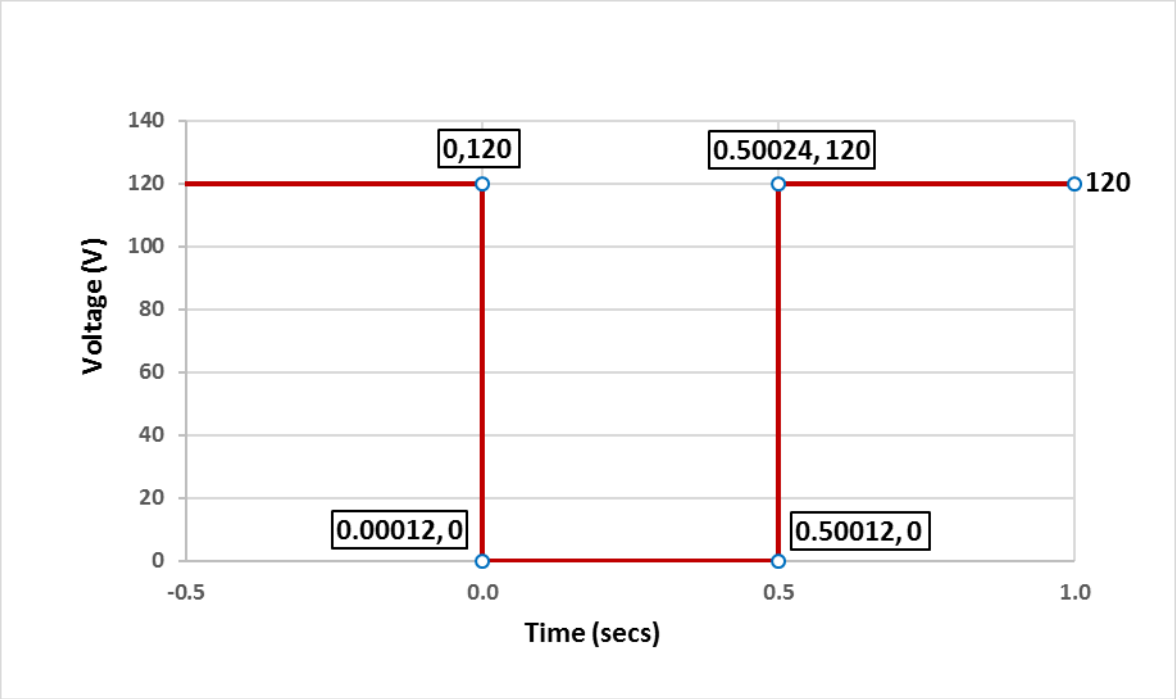


FIGURE 4.2.1-5: 120 VDC UNDERVOLTAGE TRANSIENT TEST WAVEFORM

4.2.1.2.4 EMERGENCY OPERATION

PWR120-2015V

Where specified, EPCE operation with an emergency voltage input of 95 VDC shall be verified by test.

4.2.2 28V EPCE CHARACTERISTICS

4.2.2.1 NORMAL OPERATION

4.2.2.1.1 STEADY STATE OPERATION

PWR28-2001V

Verification of EPCE operational compatibility with the steady-state voltage range shall be performed by test. Verification shall be performed by test at low and high input voltage values as specified in requirement [PWR28-2001]. EPCE shall be operated under selected loading conditions that envelop operational loading.

For 28 VDC systems, the acceptable method to demonstrate compatibility with the minimum and maximum system voltage level is to test the EPCE at a steady-state input voltage of 23 VDC (or below) and 36 VDC (or above).

The verification shall be considered successful when the test shows the EPCE operates nominally.

Rationale: EPCE undergoing susceptibility testing typically test at the low and high voltage with a voltage ripple superimposed.

4.2.2.1.2 EPCE POWER INTERFACE, NORMAL LOAD STEP TRANSIENT VOLTAGE

PWR28-2002V

Verification of compatibility with the normal load step transient at the EPS/EPCE interface shall be performed by test. Verification shall be performed by test at low and high input voltage values as specified in requirement [PWR28-2002]. EPCE shall be operated under selected loading conditions that envelop operational loading. Rate of change should be between 0.5 Volts per microsecond (V/μsec) and 1 V/μsec to prevent degradation of flight hardware (i.e. fuse fatigue).

For 28 VDC systems, EPCE should be tested by applying an input voltage transient step as shown in Figure 4.2.2-1: 28 VDC Normal Load Step-Down Transient Test and Figure 4.2.2-2: 28 VDC Normal Load Step-Up Transient Test from the nominal steady-state voltage (28 VDC) to the maximum transient levels (37 VDC) and from a steady-state voltage of 28 VDC to the minimum transient levels (21 VDC). The verification shall be considered successful when the test shows the EPCE operates nominally when input terminals are subjected to test voltages as specified in Figure 4.2.1-1 and Figure 4.2.1-2 below.

Rationale: The test conditions are at the load interface.

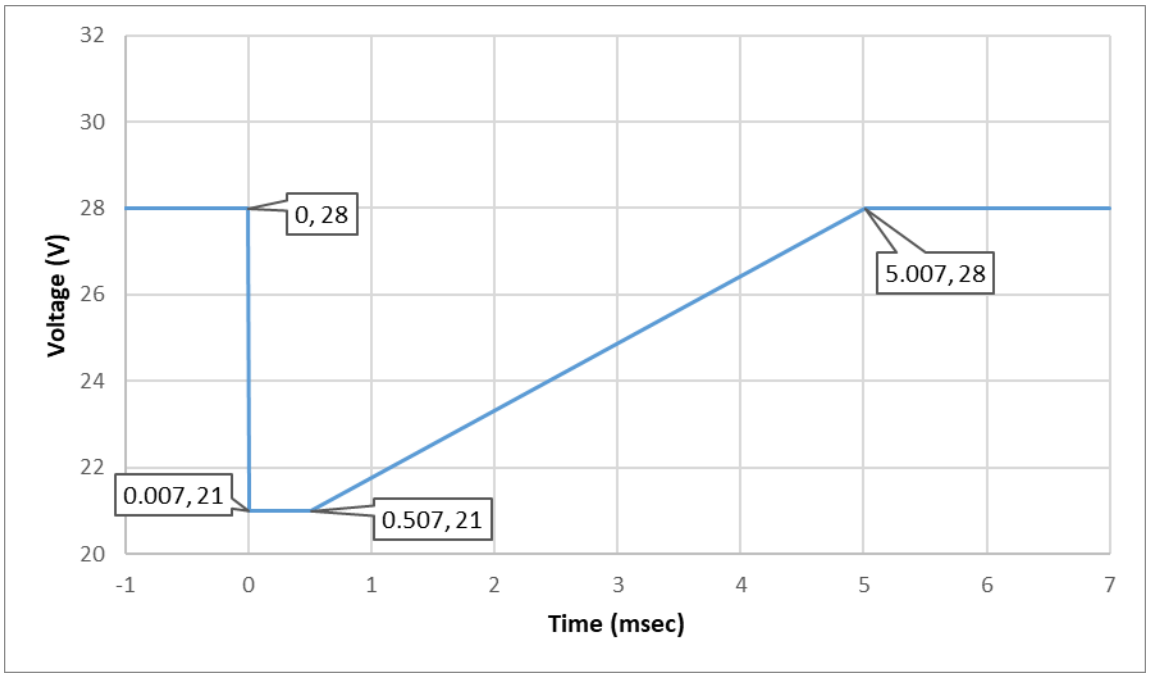


FIGURE 4.2.2-1: 28 VDC NORMAL LOAD STEP-DOWN TRANSIENT TEST

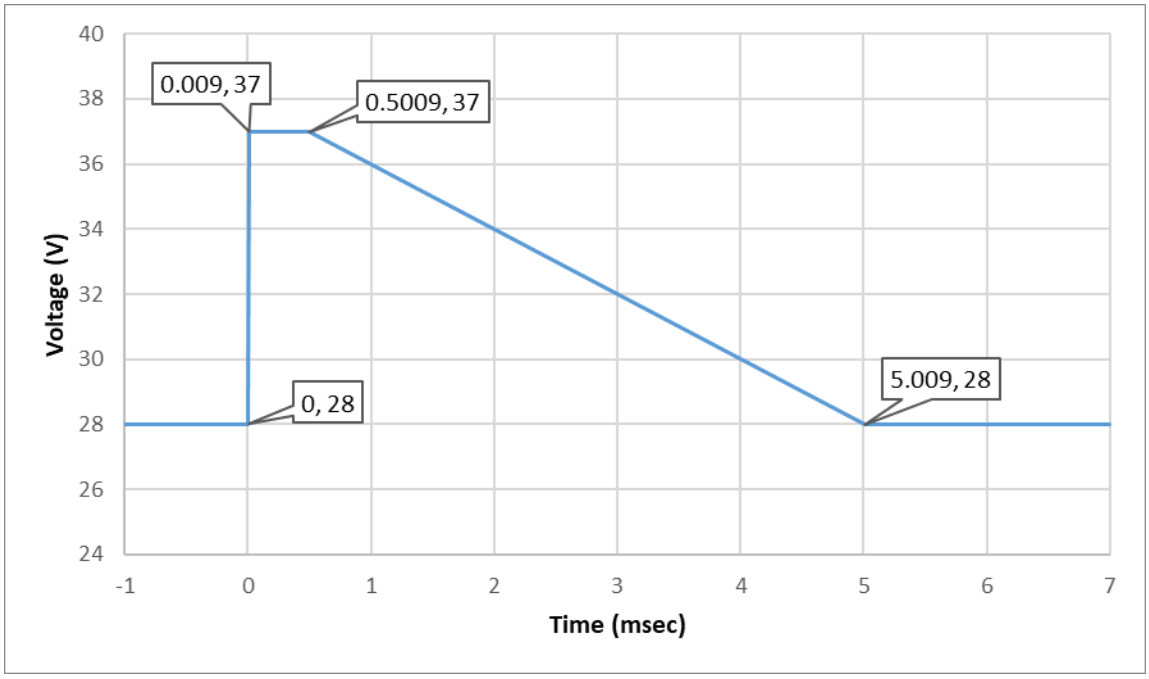


FIGURE 4.2.2-2: 28 VDC NORMAL LOAD STEP-UP TRANSIENT TEST

4.2.2.1.3 EPCE RIPPLE COMPATABILITY

4.2.2.1.3.1 EPCE, RIPPLE CURRENT

PWR28-2003V

NVR

Rationale: Verification is considered successful by successfully performing the ripple tests as defined by the EMI control document.

4.2.2.1.3.2 EPCE, RIPPLE VOLTAGE SPECTRUM

PWR28-2004V

NVR

Rationale: Verification is considered successful by successfully performing the spectrum tests as defined by the EMI control document.

4.2.2.1.4 STABILITY

4.2.2.1.4.1 LARGE SIGNAL STABILITY

PWR28-2005V

Large signal stability shall be verified by test and analysis.

A large signal stability test shall be conducted for EPCE connected to the EPS source interface. An integrated analysis shall be provided for representative maximum and

minimum load cases to demonstrate that impedance variations will not impact system stability. The input and transient response waveforms for the EPCE shall be recorded from the start of the pulse through the time when the transient diminishes to, and remains below, 10 percent of the maximum amplitude of the response. The input waveform shall be measured at the secondary side of the injection transformer.

The required test conditions may be produced using a programmable power source or the setup shown in Appendix Section E.5. Short-duration voltage pulses, as defined below shall be applied. Short-duration power-system transients are defined, as part of the Large Signal Stability requirement, as follows:

1. The rise and fall times (between 10 and 90 percent of the amplitude points) of the input voltage pulse shall be less than 1 microsecond.

2. Duration of the voltage pulse may vary between 20 microseconds and 125 microseconds in duration. In test, this shall be satisfied by applying pulses of duration of 20, 50, 80, 100, and 125 microseconds (±5 microseconds).

3. Magnitude of the voltage pulses imposed on top of the 28 ± 1.0 VDC input shall be selected such that

    a. The peak current transient is 50% above full-load current or is at the current limit of the nearest upstream switchgear.

    b. The resulting imposed voltage magnitude remains within the EPS normal load step transient limits.

The defined transient is illustrated in Figure 4.2.1-3: Large Signal Stability Test Transient and appears in series with the output of the power source as shown in Appendix Section E.5.

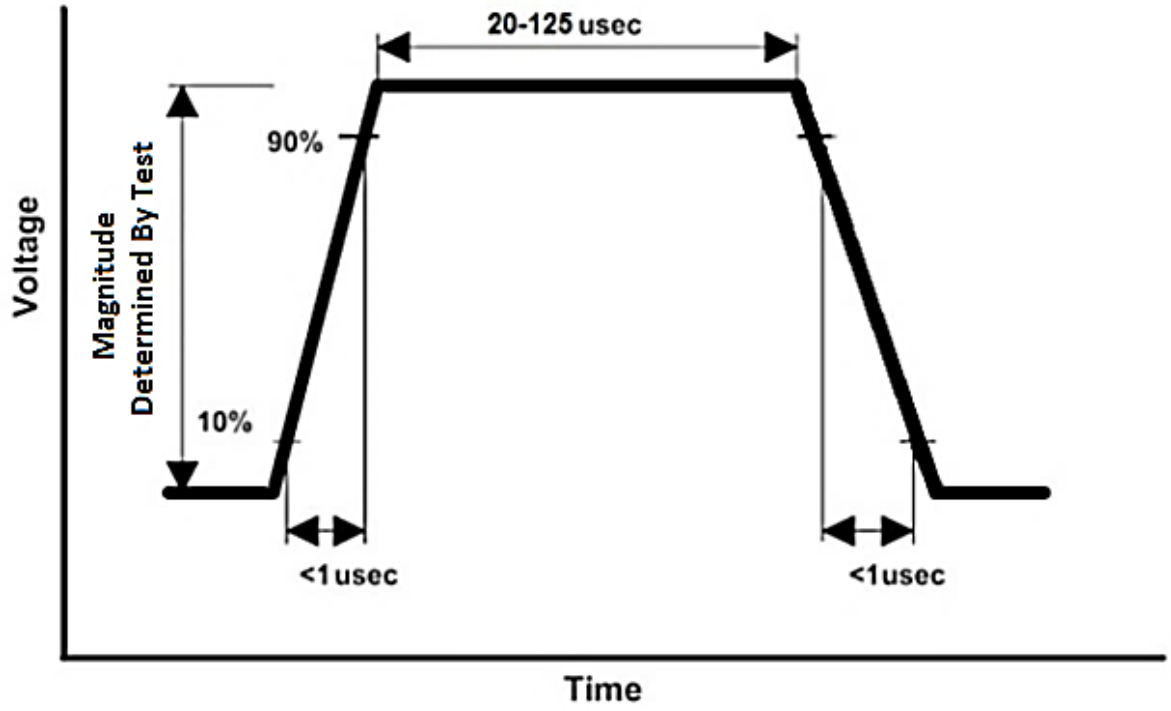


FIGURE 4.2.2-3: LARGE SIGNAL STABILITY TEST TRANSIENT

The verification shall be considered successful when results show that transient responses, measured at the input to EPCE, diminish to 10 percent of the maximum amplitude within 1.0 milliseconds and remain below 10 percent thereafter as illustrated in Figure 3.4.1-2: Large Signal Stability Transient Response. The connected EPCE shall maintain full performance as specified during the resulting transients.

For the analysis method of verification, the analysis model must be a high-fidelity time domain model (which includes the voltage and/or current control loops of the converter) in order to properly capture the voltage transient response when subjected to the large signal stability pulse.

4.2.2.1.4.2 EPCE INPUT IMPEDANCE

PWR28-2006V

Verification of EPCE input impedance shall be performed by test. See Appendix Section F. EPCE impedance shall be verified by measuring the normalized input impedance magnitude and phase at low and high input voltage values as specified in the requirement [PWR28-2006].

Rationale: This requirement needs to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same EPCE.

4.2.2.1.4.3 SMALL SIGNAL STABILITY

PWR28-2007V

Verification of EPCE small signal stability at the EPS source interface shall be performed by test and analysis. EPCE small signal stability shall be verified by calculating the complex impedance ratio of the source impedance divided by the load impedance and ensuring that it remains outside the hatched area (Forbidden Zone) shown in Figure 3.3.1-1: Nyquist Stability Criteria, from 30 Hz to 100 kHz. EPCE shall be operated under selected loading conditions that envelop operational loading. The verification shall be considered successful when the analysis supported by test data shows the Z_S divided by Z_L ratio for all defined EPCE interfaces do not cross into the Forbidden Zone defined in requirement [PWR28-2007].

Rationale: This requirement needs to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same EPCE. A basic calculation example and test setup for input impedance tests to measure both magnitude and phase curves, are described in Appendix Section F.4.

4.2.2.1.5 STARTUP AND INRUSH

4.2.2.1.5.1 CURRENT LIMITING SWITCHGEAR COMPATIBILITY

PWR28-2008V

Verification of the current limiting source compatibility shall be by test. The test shall consist of operating the device under test (DUT) being fed by current limiting switchgear that limits the current to 110% of the switchgear rating. The DUT shall not exhibit any malfunction, degradation of performance, or deviation from specified parameters when operated per requirement [PWR28-2008].

4.2.2.1.5.2 INRUSH/SURGE CURRENT TRANSIENTS

PWR28-2009V

Verification of allowable EPCE inrush and surge transient shall be performed by test and analysis using a characteristic non-current limiting source and a source that limits current to 110% of the test current as the test source. The test or analysis shall be performed as illustrated in Appendix Section E.2 to verify that the DUT inrush current during initial voltage application and surge current during DUT operation remains within the magnitude and duration limits specified in requirement [PWR28-2009] when using the non-current limiting and current limiting (110%) source. The verification shall be considered successful when the tests and analysis show that the transient remains within the limits specified in the requirement [PWR28-2008].

4.2.2.1.6 REVERSE CURRENT

PWR28-2010V

Verification of EPCE reverse current shall be performed by test and analysis. The test and analysis shall be performed on EPCE circuitry to show that, during normal operation, there are no reverse currents that will flow from the EPCE back into the EPS. The test and analysis shall be performed as illustrated in Appendix Section E.2. The analysis shall be considered successful when the tests and analysis show that no EPCE reverse current flows as specified in the requirement [PWR28-2010].

4.2.2.1.7 EPCE INPUT ISOLATION

PWR28-2011V

Verification of power source isolation shall be performed by test and analysis. EPCE equipment shall be tested to the specified limits for dielectric isolation between power sources and between power sources and chassis. Analysis of the design shall be performed to determine no single failure can cause loss of isolation.

4.2.2.2 ABNORMAL OPERATION

4.2.2.2.1 ABNORMAL REVERSE CURRENTS

PWR28-2012V

Verification of EPCE reverse current shall be performed by test and analysis. The test and analysis shall be performed as illustrated in Appendix Section E.2 on EPCE circuitry to determine the amount of current that will flow from the EPCE back into EPS during a simulated system voltage droop and EPS fault condition. The test or analysis shall be considered successful when the test and analysis show that EPCE limits reverse current flow as specified in the requirement [PWR28-2012].

4.2.2.2.2 OVERVOLTAGE SURGE

Verification of compatibility with the overvoltage surge at the EPS load interface shall be performed by test and analysis.

PWR28-2013V

For 28 VDC systems, EPCE should be tested from the nominal steady-state voltage (28 VDC) to the maximum transient levels (40 VDC), and back to the nominal steady-state voltage (28 VDC), as specified in requirement [PWR28-2013]. Figure 4.2.2-4 depicts the voltage and time steps. The test and analysis shall be performed with the EPCE subjected to an input transient with a maximum rate of change should be between 0.5 V/µsec and 1.0 V/µsec. The verification shall be considered successful when the test and analysis shows the EPCE operates nominally per the EPCE controlling documents after subjected to the overvoltage surge as specified in requirement [PWR28-2013].

Rationale: This verification of the source surge is at the EPCE interface.

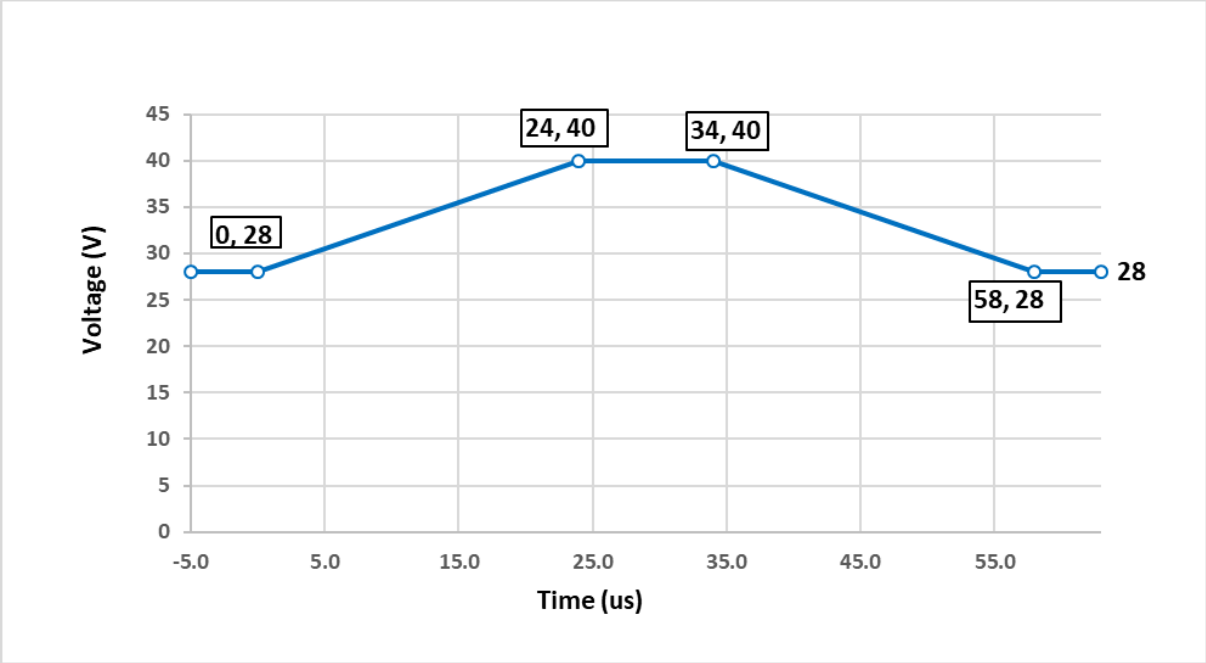


FIGURE 4.2.2-4: 28 VDC OVERVOLTAGE TRANSIENT TEST WAVEFORM

4.2.2.2.3 UNDERVOLTAGE SURGE

PWR28-2014V

The test shall be performed with the EPCE subjected to an input transient as specified in requirement [PWR28-2014]. EPCE should be tested from the steady state voltage (28 VDC) to 0 VDC and back to the steady-state voltage (28 VDC). Figure 4.2.2-5 depicts the voltage and time steps. Rate of change should be between 0.5 V/µsec and 1 V/µsec. The verification shall be considered successful when the analysis of the test results shows the EPCE operates nominally per the EPCE controlling documents after being subjected to the undervoltage surge as specified in requirement [PWR28-2014].

Rationale: This verification of the source undervoltage is at the EPCE interface.

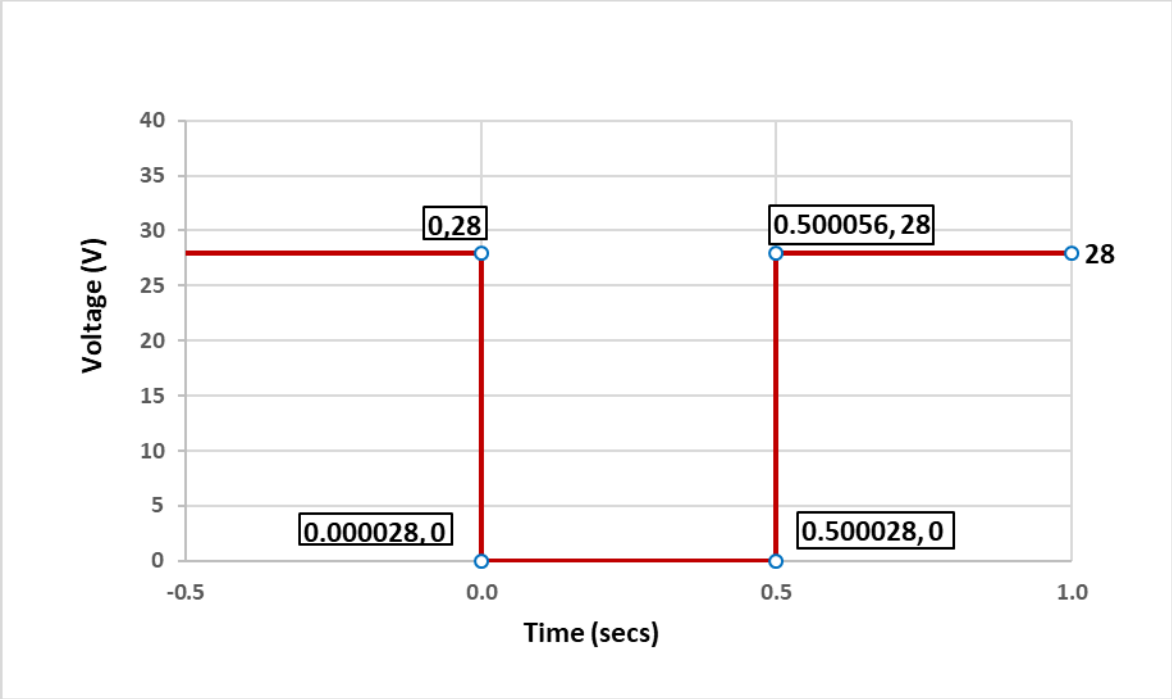


FIGURE 4.2.2-5: 28 VDC UNDERVOLTAGE TRANSIENT TEST WAVEFORM

4.2.2.2.4 EMERGENCY OPERATION

PWR28-2015V

Where specified, EPCE operation with an emergency voltage input of 18V shall be verified by test.

5 FUTURE TOPICS FOR POSSIBLE STANDARDIZATION

NA

APPENDIX A: ACRONYMS AND ABBREVIATIONS

A	Ampere
AC	alternating current
CR	Control Relay
$CR1_{CL}$	
dB	decibels
DC	direct current
DUT	device under test
e.g.	exempli gratia (for example)
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interface
EPCE	Electrical Power Consuming Equipment
EPS	Electrical Power System

ESDMD	Exploration Systems Development Mission Directorate
etc.	Et cetera
FET	Field Effect Transistor
i.e.	id Est (in other words)
Hz	Hertz
I/O	Input/Output
ISPSIS	International Space Power Systems Interoperability Standards
ISS	International Space Station
kHz	kilohertz
MΩ	Mega Ohm
MCB	Multilateral Coordination Board
MHz	megahertz
µsec	microsecond
µF	microfarad
ms	millisecond
NASA	National Aeronautics and Space Administration
NVR	No Verification Required
PEP	Portable Equipment Panel
re-gen	reverse current
rms	root-mean-square
ROD	Review of Design
SI	International System of Units
TBD	To Be Determined
TBR	To Be Resolved
V/µsec	Volts per microsecond
V	Volts
VDC	Volts direct current
Vp	Volts peak
Vrms	Volts root-mean-square
Z	Impedance
Z_L	Input impedance of the load subsystem
$\|Z_L\|$	Absolute value of Z_L
Z_S	Output impedance of the source subsystem

APPENDIX B: GLOSSARY

ABNORMAL OPERATION

Abnormal operation is that condition of the EPS wherein a fault or failure in the EPS distribution wiring, or connected loads, has occurred and the protective devices of the EPS are operating to isolate or remove the fault from the appropriate EPS interface.

BRANCH CIRCUIT

A power distribution line that delivers power from an overcurrent protection device to an electrical load device.

CLEARING TIME

The time for an overcurrent protection device to interrupt a circuit fault.

CURRENT LIMITING

The process of actively controlling the flow of electrical current to a level at, or below, a defined threshold when it might otherwise be exceeded. Also, the role of electrical protection controls that perform this function.

DETECTION TIME

The time-period between initiation of the circuit fault and initiation of the trip command to the protective device.

DISTRIBUTION SYSTEM

The means to distribute power through the power system.

ELECTRIC POWER CONSUMING EQUIPMENT

EPCE is used in this document as a generic term to refer to any piece of electrical equipment acting as a load on the Spacecraft.

ELECTRIC POWER SYSTEM

The EPS consists of the electric power generation and distribution subsystems, including all devices up to the EPCE power interface such as generators, energy storage devices, cables, switches, protective devices, converters, and regulators.

ELECTROMAGNETIC COMPATIBILITY

The ability of systems, and EPCE that are exposed to or use the electromagnetic spectrum, to operate in the operational environments without suffering unacceptable degradation or causing unintentional degradation because of electromagnetic radiation.

EMERGENCY OPERATION

Emergency operation occurs upon failure of a primary power generation/energy storage system and/or contingency cases requiring deep discharges users of electrical power.

EPS POWER INTERFACE

The EPS Power Interface is the point of connection for a fixed EPCE. For portable equipment, the EPS power interface is at the EPS receptacle.

FAULT

A condition causing overcurrent on the EPS.

FAULT CLEARING

The action in power system protection devices that disconnects a faulted line from the rest of the system.

FAULT CONTAINMENT

A mechanism to localize a circuit fault to the closest protective device.

FAULT COORDINATION

Coordinating a series of protective devices in such a way as to make sure the protective device nearest to the fault clears the fault before affecting upstream switchgear.

GROUND

Common circuit reference point considered to have 0 V.

HIGH CURRENT FAULT

A fault condition that produced very high currents generally conducting fault current through a hard, physical connection. This condition is often referred to as a "bolted fault."

HIGH IMPEDANCE FAULT

A fault condition that produces unacceptable currents but is not considered high currents. This fault is often considered the most dangerous and difficult to clear. This fault is often referred to as a "soft fault."

IMPEDANCE

Electrical impedance describes the amplitudes of the voltage, current, and phase. Impedance is the complex quantity $\bar{Z}$.

INRUSH CURRENT

Inrush current is defined as EPCE initialization current to energize loads or portions thereof. The current envelope is the total charging current in amp-seconds that starts at the instant current exceeds the rated load current of the EPCE and ends once the input current returns to the rated load current value.

INSTABILITY

Characterized by an output or internal state of a system growing without bounds.

LOCAL STABILITY

A limited measure of EPCE stability under representative (or typical) source impedance conditions.

NOMINAL RATING

An approximate value used to indicate its intended application or to differentiate it from similar devices with different ratings.

NUISANCE TRIPPING

An inadvertent interruption of an EPCE by the protection switchgear during normal operation of the load.

NORMALIZED INPUT IMPEDANCE

EPCE Input impedance curve scaled to 0 dB (1 ohm) at zero frequency.

OVERCURRENT

A situation where larger than intended electric currents exist in a circuit.

OVERCURRENT PROTECTION

The limiting of excessive circuit current by some means.

OVERVOLTAGE

A potentially hazardous condition when the voltage in a circuit or part of it is raised above the system upper design limit.

PEAK RIPPLE VOLTAGE

The absolute value of the maximum difference between the steady state and instantaneous voltage. The peak ripple voltage is the sum total peak voltage amplitude of a ripple composite, including non-periodic events that can be present on the EPS for a fixed bandwidth.

PEAK-TO-PEAK VOLTAGE

A voltage measurement of a periodic voltage waveform from the lowest well to the highest point (peak).

POWER QUALITY

Electrical characteristics that allow the system to function properly without significant loss of performance or life.

PULSED LOADS

EPCE that operates in a periodic manner with a frequency below 30 Hz.

RATED LOAD CURRENT

The maximum current draw from a load after all start-up or mode change transients have settled out.

RATED POWER

The nominal output power for EPS branch circuits or power consumption of an EPCE.

REPRESENTATIVE LOAD

EPCE that can be either constant power or resistive that stresses the power source to verify performance envelope compliance.

REVERSE CURRENT

Direct current flowing in the opposite direction from the intended circuit design. For loads, this can be created from the energy discharge of a circuit due to counter

electromagnetic force due to regenerative loads (such as motor controllers or actuators) or under a fault condition upstream of the load power interface.

RIPPLE CURRENT

Ripple current is a time-varying current waveform superimposed on a purely DC current.

RIPPLE VOLTAGE

Ripple voltage is a time-varying voltage waveform superimposed on a purely DC voltage.

RIPPLE VOLTAGE AMPLITUDE

Ripple voltage is the rms value of all AC voltage components that are superimposed on the steady-state DC voltage.

RIPPLE VOLTAGE SPECTRUM

The frequency distribution of ripple voltage components.

SHORT CIRCUIT

Abnormal low impedance/resistance connection between nodes of an electrical circuit at different voltages.

SINGLE-POINT GROUND

Single-Point Ground is a single ground reference to structure.

STABILITY

The quality of electrical device operation wherein key characteristics resist deviation from intended values under both static and dynamic conditions.

SURGE CURRENT

Surge current is defined as a transient, or pulsed, current, due to operation of an EPCE that is greater than the average over any interval of time.

SWITCHGEAR

The combination of electrical/electronic disconnects or fuses used to operate/isolate electrical equipment. Switchgear can be designed to both operate and protect (clear circuit faults) equipment.

TRANSIENT RESPONSE

A disturbance in an electrical system brought about by a sudden change of load.

TWO-WIRE

An electrical distribution system using separate supply and return conductors to supply electrical power to an EPCE.

TRIP TIME

The time for an overcurrent protection device to interrupt a circuit fault.

VOLTAGE DROOP

The reduction in output voltage due to a fault or failure.

VOLTAGE SPECTRUM

A graph of individual voltage intensity components plotted against frequency.

APPENDIX C: OPEN WORK

Table 1 lists the specific To Be Determined (TBD) items in the document that are not yet known. The TBD is inserted as a placeholder wherever the required data is needed and is formatted in bold type within brackets. The TBD item is numbered based on the section where the first occurrence of the item is located as the first digit and a consecutive number as the second digit (i.e., <TBD 4-1> is the first undetermined item assigned in Section 4 of the document). As each TBD is solved, the updated text is inserted in each place that the TBD appears in the document and the item is removed from this table. As new TBD items are assigned, they will be added to this list in accordance with the above described numbering scheme. Original TBDs will not be renumbered.

TABLE 1: TO BE DETERMINED ISSUES

TBD	Section	Description

Table 2 lists the specific To Be Resolved (TBR) issues in the document that are not yet known. The TBR is inserted as a placeholder wherever the required data is needed and is formatted in bold type within brackets. The TBR issue is numbered based on the section where the first occurrence of the issue is located as the first digit and a consecutive number as the second digit (i.e., <TBR 4-1> is the first unresolved issue assigned in Section 4 of the document). As each TBR is resolved, the updated text is inserted in each place that the TBR appears in the document and the issue is removed from this table. As new TBR issues are assigned, they will be added to this list in accordance with the above described numbering scheme. Original TBRs will not be renumbered.

TABLE 2: TO BE RESOLVED ISSUES

TBR	Section	Description

APPENDIX D: SYMBOL DEFINITIONS

<reserved>

APPENDIX E: TEST METHODS

E.1 Input Impedance Measurements

EPS source interface is the point where user loads will be connected to the power system. The test described in this section is the suggested test setup to measure load impedance at the EPS source interface. It is important to understand that the load

impedance measurement test setup will include a simulated source and the EPCE under test. The EPCE input impedance can be measured by injecting an AC signal to the system using either of two methods: series voltage injection and parallel current injection.

Generally, the load input impedance is greater than the source output impedance in magnitude. Figure E.1-1, Test Setup for Impedance Measure Using Series Voltage Injection, shows a typical test setup for series voltage injection method. This method works better for measuring load input impedance because most of the injected voltage signal is applied to the high impedance in the load side. The figure shows the measurement of load impedance at the input terminals of an EPCE. Note: it is recommended to place the load on a non-conductive surface when performing this test to avoid effects caused by any common mode capacitance within the load.

Analysis Steps:

1) Determine the base DC input impedance, Z_{rated}, of the EPCE at the worst-case operating condition. This condition will normally be operation at minimum input voltage and maximum load of the EPCE. V_{rated} is the rated voltage of the EPCE and I_{rated} is the rated steady-state EPCE current.

   i) $Z_{rated} = V_{rated} / I_{rated} = (V_{rated})^2 / P_{rated}$

2) Obtain Bode Plots for the magnitude and phase of the impedance versus frequency for each test condition.

3) Determine per unit magnitude, $Z_{perunit}$, by dividing the magnitude values of each plot by the value of Z_{rated} obtained in step 1. The resulting plots will represent the magnitudes in per unit ohms after converting to dB ohms.

   i) $Z_{perunit} = Z_{actual} / Z_{rated}$

   ii) $Z_{perunit}$ dB Ohms = 20 X log ($Z_{perunit}$)

   NOTE: Other equivalent test support equipment can be used for the impedance test.

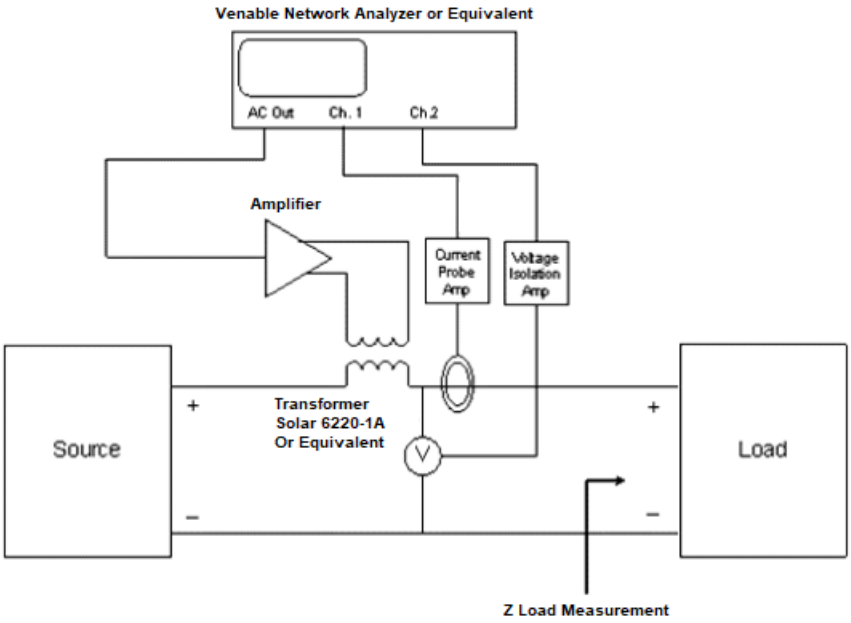


Figure 4.2.2-1: Test Setup for Impedance Measure Using Series Voltage Injection

Example 1 - *Figure 4.2.2-2: Example Input Impedance Magnitude of* Load, shows the input impedance magnitude of a load which is rated at 873 W. The base impedance, $Z_{rated} = 98^2 / 873 = 11$ ohms. The per-unit impedance (Figure E.1-3, Example $Z_{perunit}$ Input Impedance Magnitude of Load) on this load is obtained by dividing the actual impedance magnitude, Z_{actual}, (*Figure 4.2.2-2: Example Input Impedance Magnitude of* Load) by Z_{rated} and converting the results into dB (dB Ohms = $20*\log(Z_{perunit})$). Figure 4.2.2-3: Example $Z_{perunit}$ Input Impedance Magnitude of Load, also compares the per-unit input impedance of this load to the requirement.

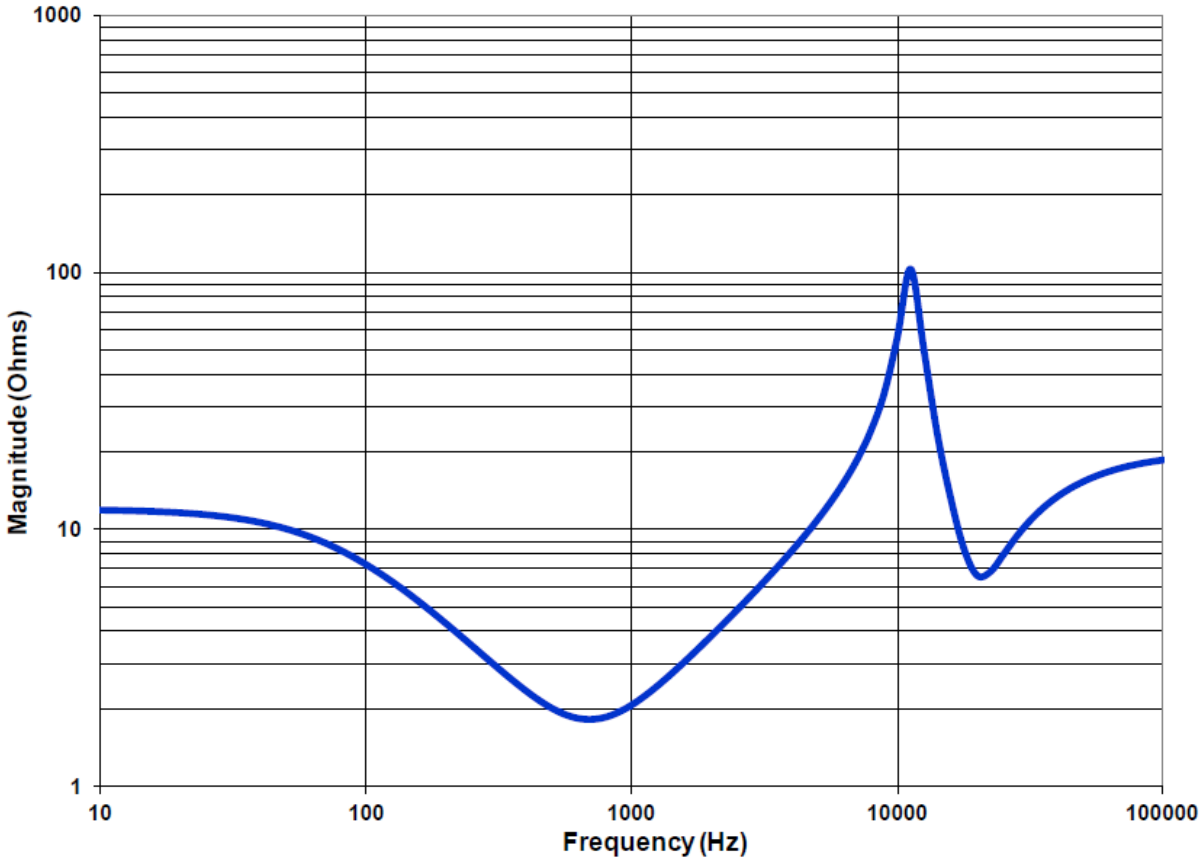


Figure 4.2.2-2: Example Input Impedance Magnitude of Load

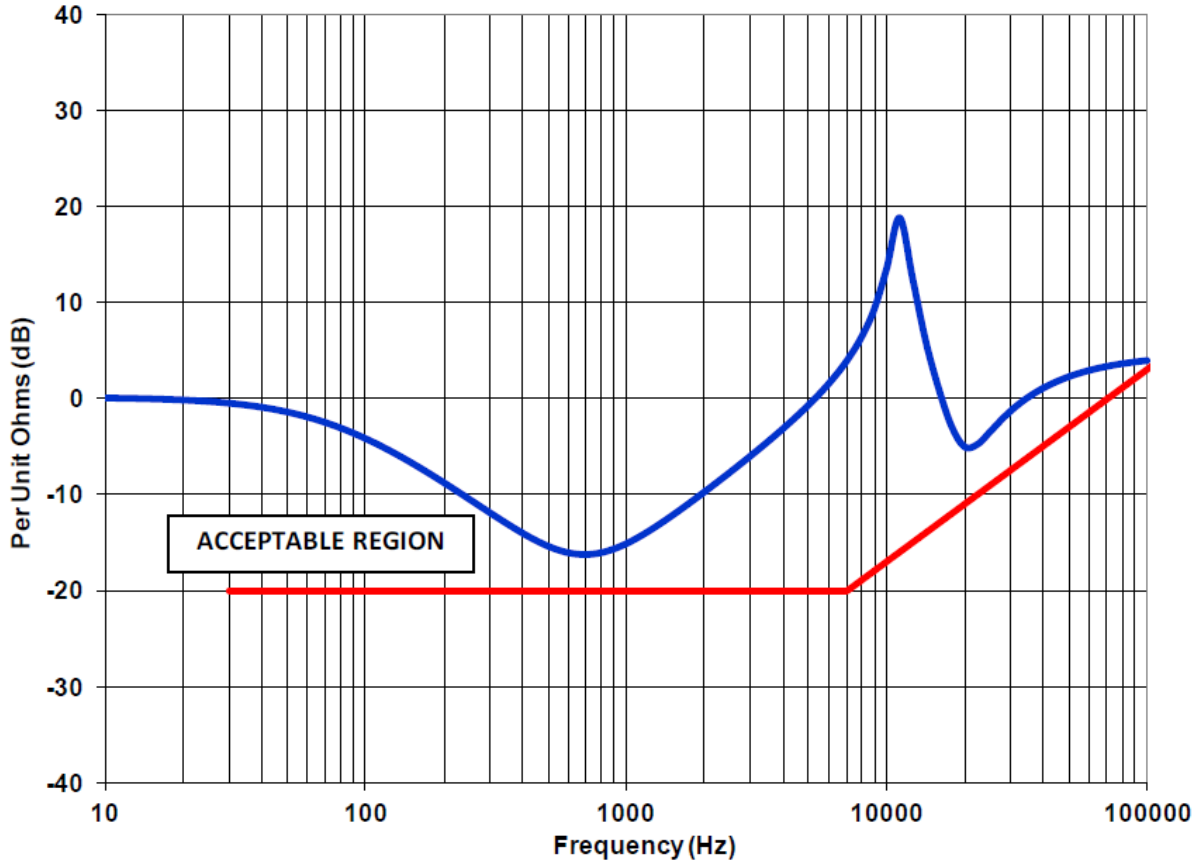


Figure 4.2.2-3: Example $Z_{perunit}$ Input Impedance Magnitude of Load

E.2 Load Steady-State, Inrush, Surge and Reverse Current

Figure 4.2.2-1, shows a typical test setup for measuring voltage and current at the EPCE input terminals. Other test support equipment can be used. The power supply output ratings must be high enough that the measured surge currents are not limited by its output capacity for the load and inrush test. The power supply for reverse current must be output current limiting with adequate capacity to supply steady state load current.

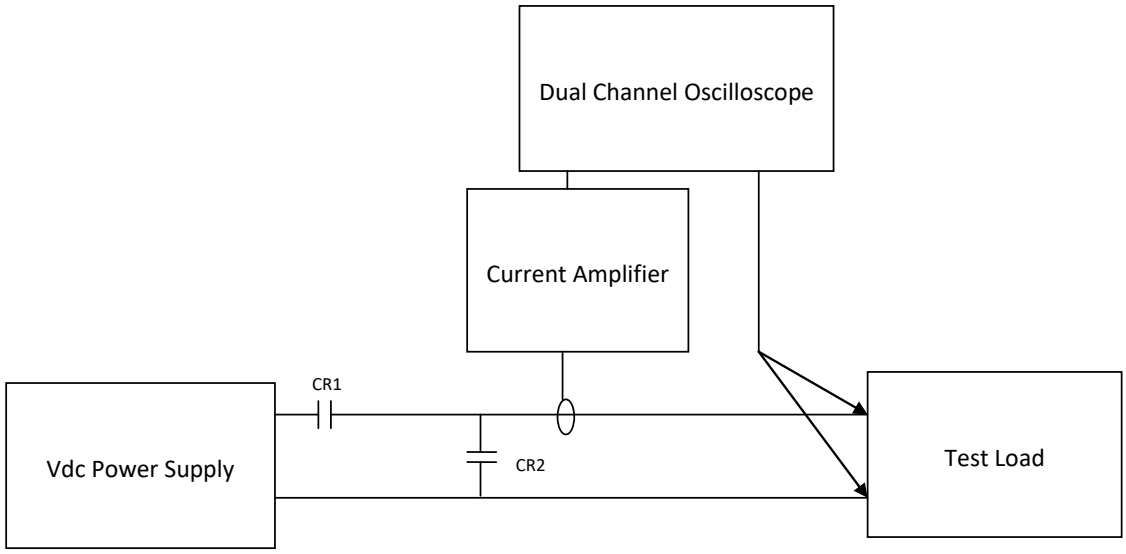


Figure 4.2.2-1: Typical Test Setup For Inrush, Surge, And Reverse Current Measurements

NOTE: A stiff power source is required for this test. Capacitance may be added to stabilize the source.

The voltage sag, δV due to transient inrush current at the input to the DUT should meet the following inequality:

$$\delta V \le (V_{nominal} - V_{minimum}) \bullet \sqrt{\left(\frac{I_{SS}}{I_{bus}}\right)}$$

Where,

$V_{nominal}$ = nominal bus voltage

$V_{minimum}$ = specified minimum bus voltage

I_{SS} = DUT steady-state current draw

I_{bus} = power bus maximum steady state draw

E.3 TYPICAL RATED LOAD, INRUSH, OPERATION WITH CURRENT LIMITING SWITCHGEAR AND NORMAL REVERSE CURRENT TESTING PROCEDURES

E.3.1 RATED LOAD AND INRUSH CURRENT

Current limiting devices will not be present in the line between the power supply and the EPCE under test.

a) With relay CR1 open, energize the power supply.

b) With the DUT configured to draw maximum power, close the CR1 relay to energize the DUT, record the inrush current and voltage.

c) Allow sufficient time for a steady state condition; record the load current.

d) De-energize the power supply; record the normal reverse current.

e) Measure and record the current and voltage waveforms.

E.3.2 OPERATION WITH CURRENT LIMITING SWITCHGEAR

a) Replace CR1 with a relevant current limiting device ($CR1_{CL}$) in the line between the power supply and the EPCE under test.

b) With $CR1_{CL}$ open, energize the power supply.

c) With the DUT configured to draw maximum power, close the $CR1_{CL}$ to energize the DUT, record the inrush current.

d) Allow sufficient time for a steady state condition; record the rated load current.

e) De-energize the power supply; record the normal reverse current.

f) Measure and record the current and voltage waveforms.

E.3.3 REVERSE CURRENT DURING A CIRCUIT FAULT

It is recommended that CR1 and CR2 be solid state switches with the capability to source and sink the required currents.

a) With relay CR1 open, energize the power supply.

b) With the DUT configured to draw maximum power, close the CR1 relay to energize the DUT and allow the DUT to reach steady state operation.

c) Open CR1 and Close CR2 – This transition must be within 5 µs.

d) Measure and record the current and voltage waveforms.

E.3.4 ANALYSIS

The inrush and reverse current waveform may be digitized to allow computation of the ampere-seconds value by numerical integration. The resulting input current and voltage waveforms, to the EPCE, can be used to validate computer models used in analysis.

E.4 Source Impedance Measurement

The tests described in this section are suggested test setups to measure EPS source impedance. A single test at nominal load may be adequate for passive sources such as a battery or fuel cell. Active sources such as DC/DC converters, usually require tests over a range of load currents (<10% load to full load).

Figure E.3.4-1 illustrates a source impedance test method. A network analyzer is connected to measure the AC components of the source voltage and output current. The analyzer output provides a signal to modulate the load current. Either square wave or sine wave modulation may be used, depending on the network analyzer used.

Figure E.3.4-1 illustrates a source impedance test method. A network analyzer is connected to measure the AC components of the source voltage and output current. The analyzer output provides a signal to modulate the load current. Either square wave or sine wave modulation may be used, depending on the network analyzer used.

If the audio amplifier and transformer shown in Figure E.3.4-1: Series Voltage Injection Source Impedance Test Configuration, are available, the Parallel Current Injection method may be used. The amplifier output modulates the load current and the voltage and current sensors provide input to the analyzer.

Test Steps:

1. Configure the network analyzer to calculate $Z_{source} = V_{ac}/I_{ac}$, where V_{ac} and I_{ac} are the AC components of the measured voltage and current.

2. Set the resistive load to the desired value.

3. Obtain Bode plots for the magnitude and phase of the impedance versus frequency for each load condition.

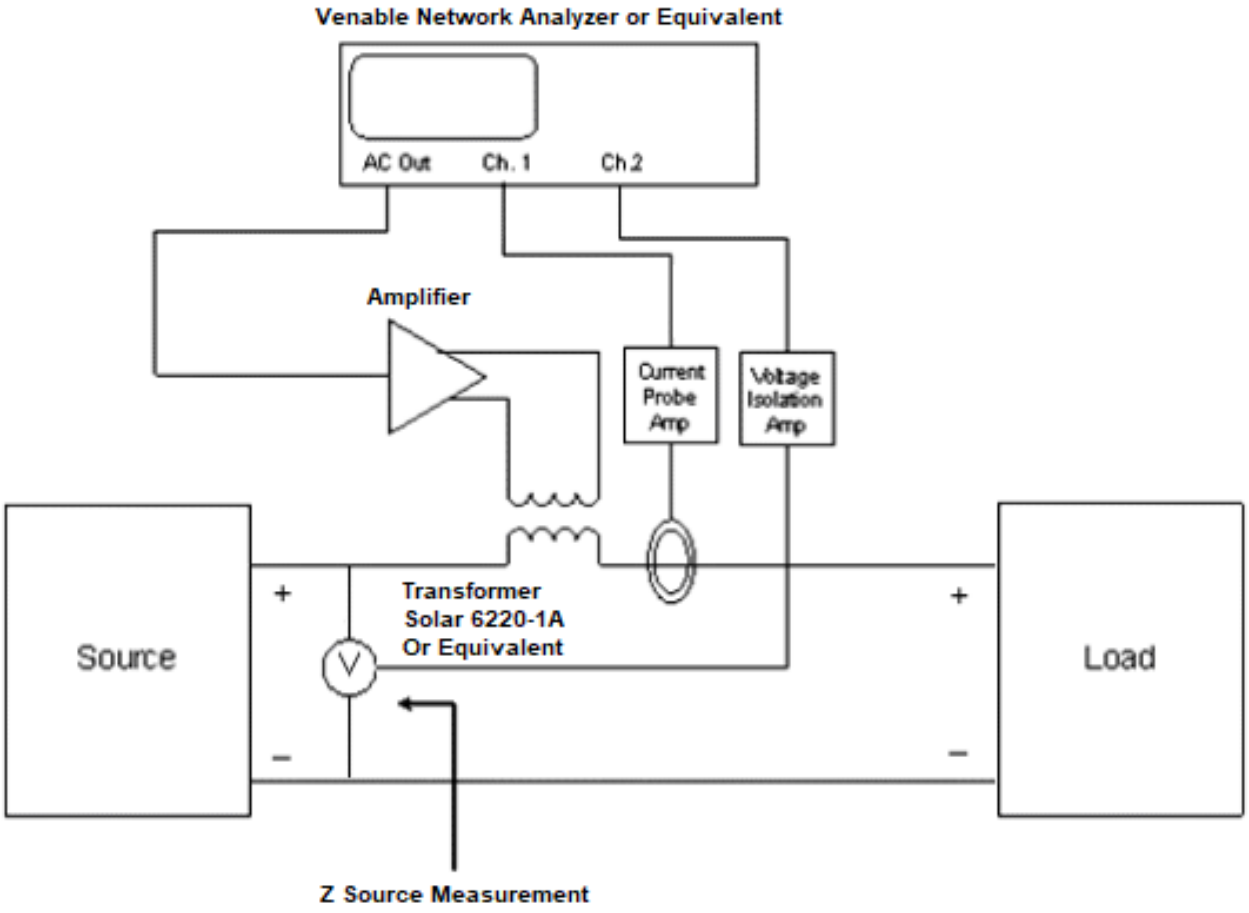


Figure E.3.4-1: Series Voltage Injection Source Impedance Test Configuration

E.5 LARGE SIGNAL STABILITY

A typical large signal stability test setup is shown Figure E.3.4-1: Large Signal Stability Test Configuration. The pulse generator/amplifier, with source impedance of less than 0.2 ohms from 100 Hz to 10 kHz, must provide power to the 2-ohm load of the primary side of the pulse transformer. Short-duration power-system transients per [PWR120-2005V] and [PWR28-2005V] should be applied. An alternate test set-up can be the same as used for the normal and abnormal voltage transient tests.

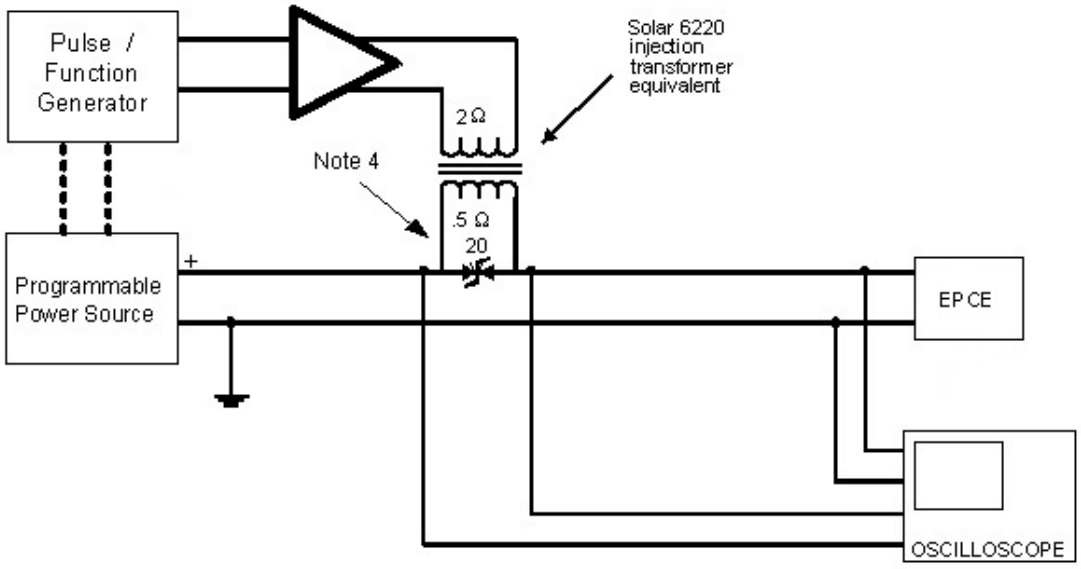


Figure E.3.4-1: Large Signal Stability Test Configuration

NOTE:

1. The output of the pulse generator must be applied to the transformer through a drive amplifier that has less than 0.2-ohm output (source) impedance from 100 Hz to 10 kHz.
2. The drive amplifier should be capable of delivering at least 75 watts into a 4-ohm load.
3. A differential probe is used if the scope is grounded.
4. Pulse generator, injection transformer and Zener diode may require adjustment to generate the test pulses and to protect the EPCE under test.
5. The power source should be representative of the power environment.

Specifications will denote what is required to make the source representative. General Discussion

APPENDIX F: Power Quality

Power quality, as defined, includes ripple voltage, time transient system response, and bus voltage operation range. Nominal DC voltage is generally not considered power quality but more of a system definition. The time varying nature of power quality affects this nominal voltage to create the "Steady-state Normal" voltage range used within this standard. EPCE designers must address the ripple voltage effects and contributions from the attached loads, load modulations, and radiated susceptibility. Switching of power sources, distribution switchgear, converters, and regulators provide a base "source" ripple voltage that is inherent with the power system. The next source of ripple is reflective ripple from the loads themselves back onto the power system. Load modulation ripple due to loads that are modulated or pulsed, repeatedly switched off to on, whether by nature or due to external effects, when large enough, can cause voltage overshoot and undershoot when operating. An example of modulated loads can be the docking mechanisms used for vehicle docking. Finally, ripple voltage due to radiated susceptibility can be impressed on the power system from a radiated source where the influences are dependent on the geometry of the power system.

To minimize unnecessary designer constraints, the system frequency spectrum was adopted as a worst-case design benchmark for ripple voltage.

F.1 PORTABLE LOADS

Special considerations are needed by the electric power consumer user when using an extension cord and multi-outlet power strips. The power quality at this interface can be adversely affected by misapplication of this requirement. Loads with high inrush current, high peak power to average power ratio, and high current ripple amplitude can adversely affect the power quality at this interface by degrading electric power characteristics. Power quality problems are exacerbated when multiple portable loads are connected to a single multi-outlet power strip, with loads not coordinated, causing voltage sag, current limiting, and voltage dropout, essentially a loss of power quality. The total aggregate electrical loading when using a multi-outlet power strip should be taken into consideration with respect to the upstream power feed. Voltage droop, voltage dropout, and the normal/abnormal system transients can be associated with this interface when loads are misapplied. The EPCE connected to this interface need to be designed to operate through or not suffer damage or cause an unsafe condition due to this abnormal power quality.

F.2 Capacitive Loads

Large capacitive input filters or loads can have a stabilizing effect on the EPS, although excessive capacitance can create voltage droop during power-up. Loads with large input capacitance must be coordinated with protective switchgear. The user must ensure that these capacitance limits are not exceeded on a per channel basis.

F.3 Inductive Loads

Large inductive loads, such as large solenoids, stepper motors, valves, contactors, etc., require voltage transient suppression to control EMC emissions and reverse energy requirements. Large inductive loads when combined with constant power converters can cause output tripping when the current demand is not coordinated with the protective switchgear.

F.4 STABILITY CRITERIA – SMALL SIGNAL STABILITY APPROACH

A typical cause of system instability is negative impedance load. This negative impedance occurs in systems that frequently include constant power loads. As long as a negative impedance load is powered by an ideal voltage source (with very low output impedance), the system is stable. However, in cases in which the load is powered by a non-ideal source whose output impedance amplitude is larger than the negative load impedance, the whole system may become unstable.

For checking small-signal system stability, the concept of an impedance criterion was adopted by the designers of filter-switching regulators with input filters. The concept was found to be useful in analyzing the stability of distributed power systems at the interface between the source subsystem and the load subsystem. At the system-level, impedance specifications for each subsystem can be defined based on the requirements for system stability. At the component level, knowledge of the Input/Output (I/O) impedance characteristics of a module/subsystem is required to meet the specifications for system stability.

Figure E.3.4-1: Series Integration of Two Subsystems shows a system with source and load impedances. Z_S is the output impedance of the source subsystem; Z_L is the input impedance of the load subsystem.

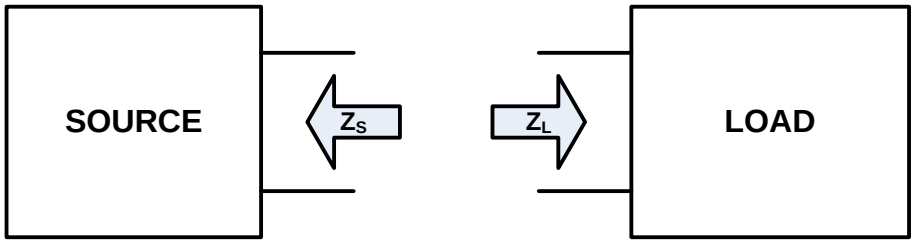


Figure E.3.4-1: Series Integration of Two Subsystems

When the source is connected to the load, the parallel combination of Z_S and Z_L is given by:

$$Z = \frac{Z_S \cdot Z_L}{Z_S + Z_L} = \frac{Z_S}{\frac{Z_S}{Z_L} + 1}$$

If $|Z_S| < |Z_L|$ for all frequencies, then, the system is stable. When $|Z_S| > |Z_L|$, further analysis is needed to determine system stability. The Nyquist criterion can then be applied to determine a less conservative criterion that assures system stability.

According to the Nyquist criterion, small-signal system stability can be determined by whether the curve of Z_S/Z_L circles the (-1,0) in the S-plane as shown in Figure F.5-2, Forbidden Zone for Z_S/Z_L.

A forbidden region on this diagram establishes a system stability margin.

By keeping Z_S/Z_L out of the forbidden region as shown in the figure, small signal stability can be assured.

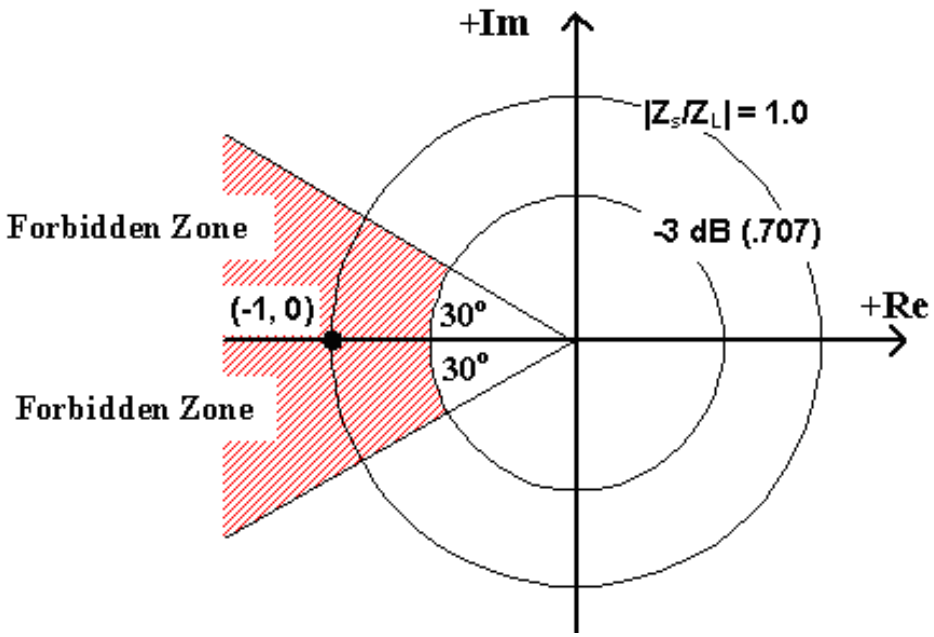


Figure E.3.4-2: Forbidden Zone for Z_S/Z_L